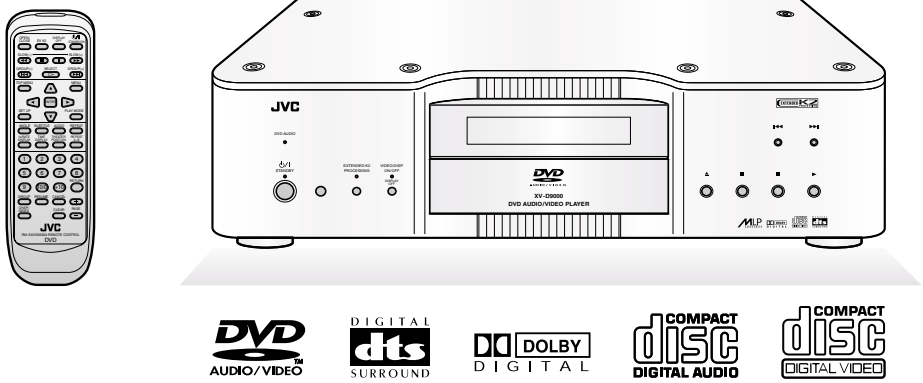
JVC

SERVICE MANUAL

DVD AUDIO/VIDEO PLAYER

XV-D9000

Area Suffix
E ------- Continental Europe

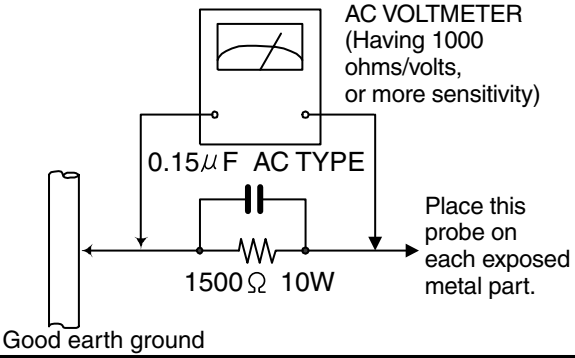


Contents

No.A0007
Apr. 2001

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after reassembling.
5. Leakage current check (Electrical shock hazard testing)
   After reassembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet , particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
     Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and measure the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ ***CAUTION*** **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.1. Grounding to prevent damage by static electricity

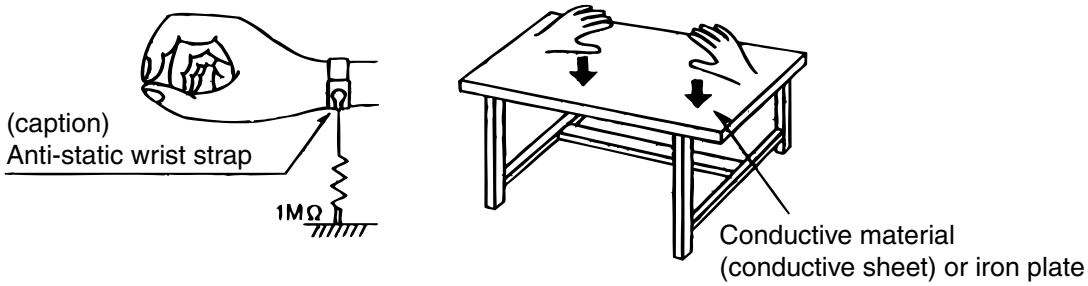
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.

3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Dismantling and assembling the traverse unit

1. Notice regarding replacement of optical pickup

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs to the optical pickup or connected devices.

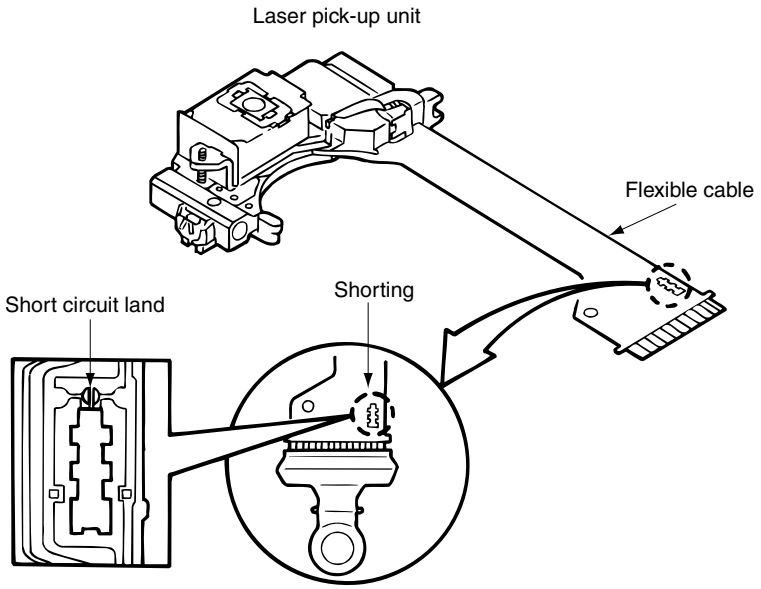
(Refer to the section regarding anti-static measures.)

1. Do not touch the area around the laser diode and actuator.

2. Do not check the laser diode using a tester, as the diode may easily be destroyed.

3. It is recommended that you use a grounded soldering iron when shorting or removing the laser diode.
Recommended soldering iron: HAKKO ESD-compatible product

4. Solder the land on the optical pickup's flexible cable.
- Note : Short the land after shorting the terminal on the flexible cable using a clip, etc., when using an ungrounded soldering iron.
- Note : After shorting the laser diode according to the procedure above, remove the solder according to the text explanation.



Important for Laser Products

1.CLASS 1 LASER PRODUCT

2.DANGER : Invisible laser radiation when open and inter lock failed or defeated. Avoid direct exposure to beam.

3.CAUTION : There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.

4.CAUTION : The compact disc player uses invisible laser radiation and is equipped with safety switches which prevent emission of radiation when the drawer is open and the safety interlocks have failed or are de feated. It is dangerous to defeat the safety switches.

5.CAUTION : If safety switches malfunction, the laser is able to function.

6.CAUTION : Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

⚠ ***CAUTION*** **Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.**

VARNING : Osynlig laserstrålning är denna del är öppnad och spårren är urkopplad. Betrakta ej strålen.

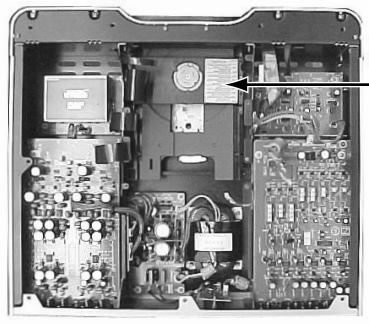
VARO : Avattaessa ja suojalukitus ohitettaessa olet alttiina näkymättömälle lasersäteilylle.Älä katso säteeseen.

ADVARSEL : Usynlig laserstråling ved åbning , når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

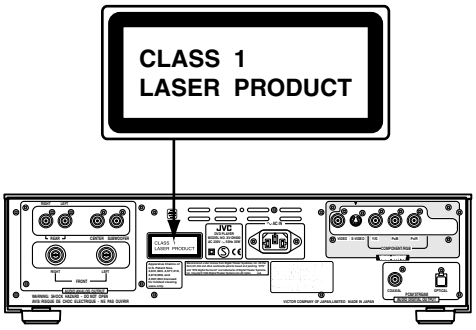
ADVARSEL : Usynlig laserstråling ved åpning,når sikkerhetsbryteren er avslott. unngå utsettelse for stråling.

REPRODUCTION AND POSITION OF LABEL and PRINT

WARNING LABEL and PRINT



CAUTION	- LASER RADIATION WHEN OPEN. DO NOT STARE INTO BEAM.
ATTENTION	- RAYONNEMENT LASER EN CAS D'OUVERTURE. NE PAS REGARDER DANS LE FAISCEAU.
VORSICHT	- LASERSTRAHLUNG, WENN ABDECKUNG GE..FFENET. NICHT IN DEN STRAHL BLICKEN.
ADVARSEL	- LASERSTR LING VED BNING. SE IKKE IND I STR LEN.
ADVARSEL	- LASERSTR LING N R DEKSEL PNES. STIRR IKKE INN I STR LEN.
VARNING	- LASERSTR LNING N R DENNA DEL R ..PPNAD. STRRA EJ IN I STR LEN.
VARO!	AVATTAESSA OLET ALTTIINA LASERS TEILYLLE. L TUIJOTA S TEESEEN.
注意	- 当打开这里会出现激光，请不要直视激光。
注意	- ここを開くとレーザー光が出ます。レーザー光をのぞき込まないでください。



Disassembly method

<Main body>

■ Removing the top panel(See Fig.1)

1.Remove the eight screws **A** by hexagonal driver attaching the top panel.

2.A top panel is lifted up and it is removed.

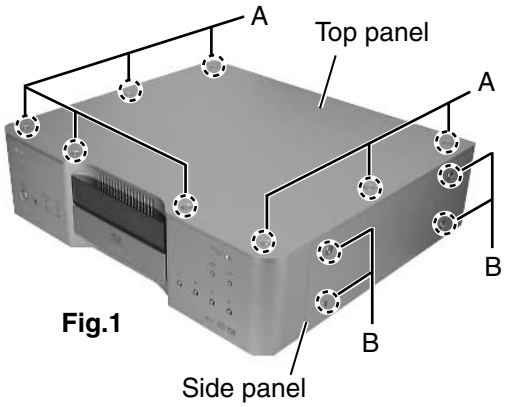


Fig.1

■ Removing the side panel(See Fig.1)

1.Remove the four screws **B** by hexagonal driver attaching the side panel.

2.The left side also similarly removes the side panel.

■ Removing the front panel assembly (See Fig.1~5)

*Prior to performing the following procedure, remove the top panel.

1.The bottom of the main body is done up.

2.A minus driver is inserted in the incision part at the center of the bottom, the bar in the interior of the incision part is moved in the direction of the arrow of Figure 2, and the tray is drawn out forward.

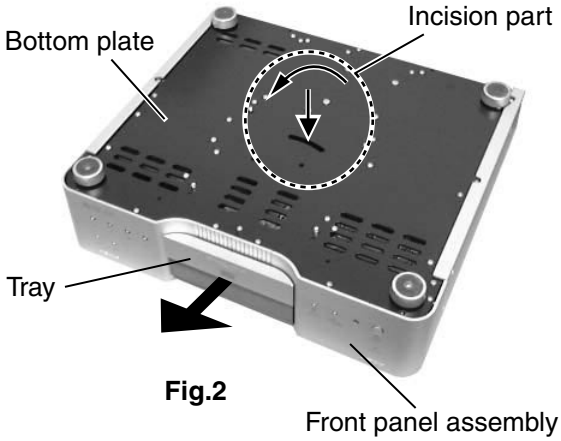


Fig.2

3.Hook **a** which connects the tray covers to the tray is removed by a minus driver etc. , the tray cover is pushed downward, and removes.

4.Remove the six screws **C** attaching the front panel assembly.

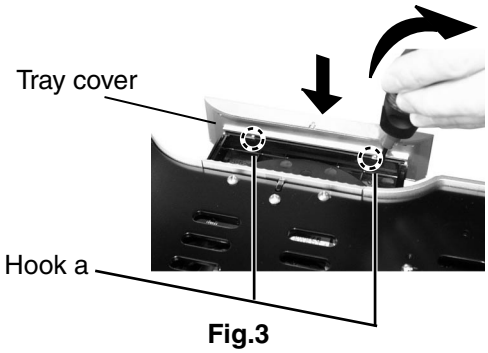


Fig.3

5.The top of the main body is done up.

6.Remove the eight screws **D** attaching the front panel assembly from the upper side of main body.

7.Disconnect the wire from connector CN507 on the main board and CN981 on the power supply board.

8.It comes off when the front panel assembly is drawn out forward.

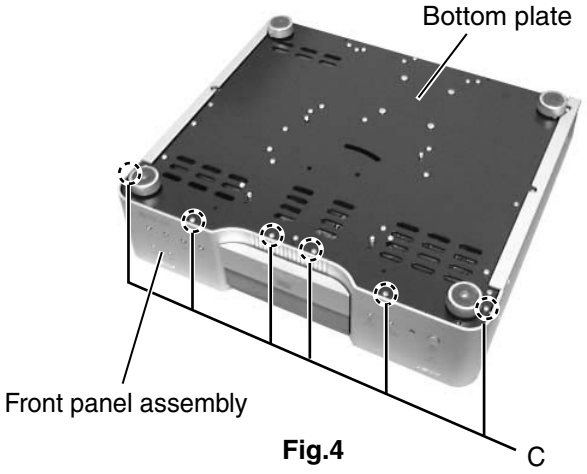


Fig.4

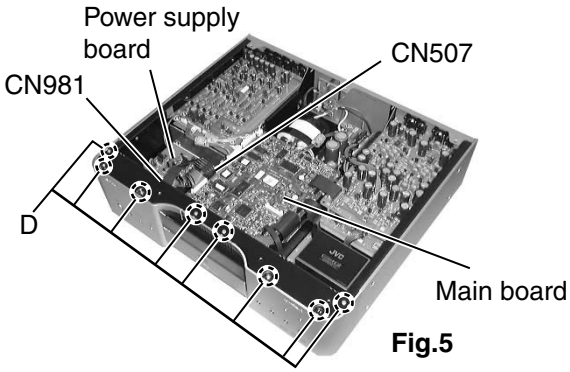


Fig.5

■ Removing the rear cover(See Fig.6~8)

*Prior to performing the following procedure, remove the top panel.

1.Remove the eighteen screws **E** attaching the rear cover from back of the main body.

2.Remove the three screws **F** attaching the bottom plate from back of the main body.

3.Solder on the power supply board is removed by three places.(See Fig.8)

4.Remove the two screws **G** attaching the AC socket.

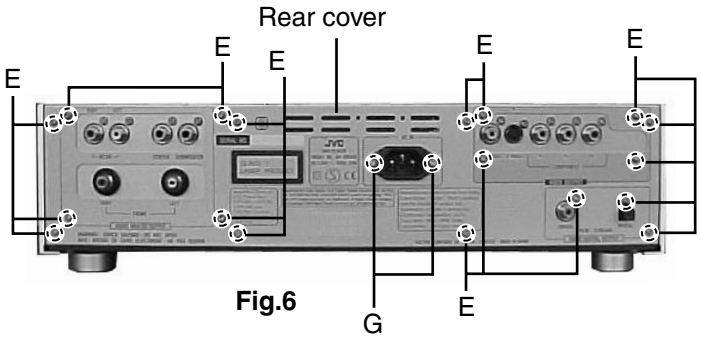


Fig.6

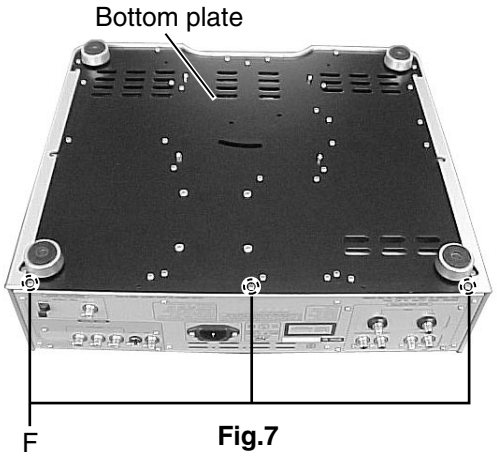


Fig.7

■ Removing the main board(See Fig.8)

*Prior to performing the following procedure, remove the top panel.

1.Remove the four screws **H** attaching the main board.

2.Disconnect the connector from CN101, CN103,CN504,CN505,CN501,CN502, CN506,CN507 on the main board.

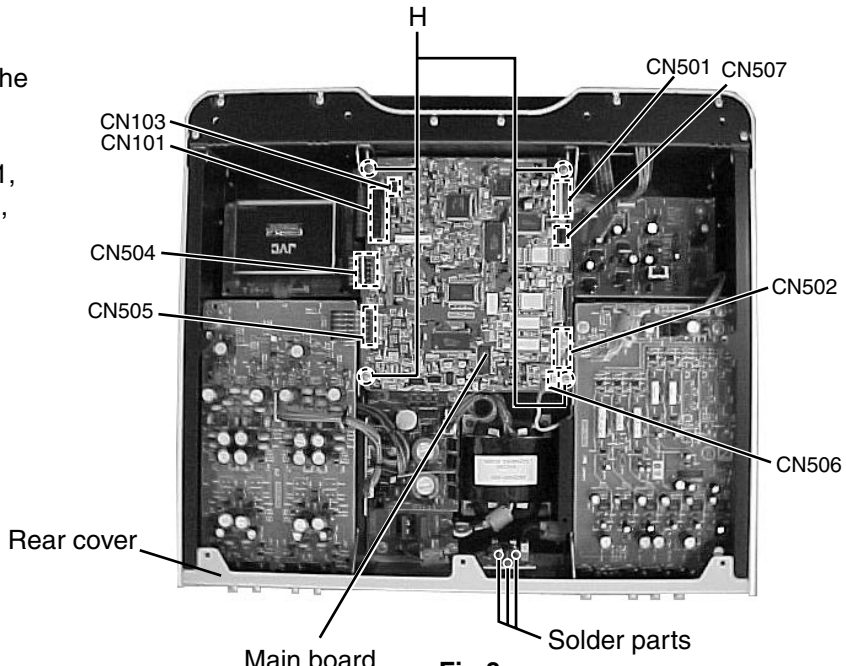


Fig.8

■ Removing the DVD mechanism assembly (See Fig.9~11)

*Prior to performing the following procedure, remove the top panel and main board.

1.Remove the four screws **I** attaching the DVD mechanism assembly cover, and DVD mechanism assembly cover lifted up and it is removed.

2.The bottom of the main body is done up.

3.Remove the four nut **J** attaching the DVD mechanism assembly

4.The top of the main body is done up.

5.Remove the four screws **K** attaching the DVD mechanism assembly.

6.It is removed while lifting the DVD mechanism assembly backward while noting the card wire.

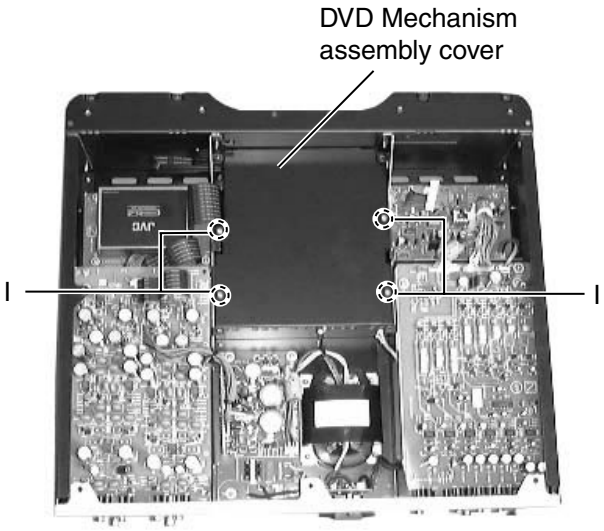


Fig.9

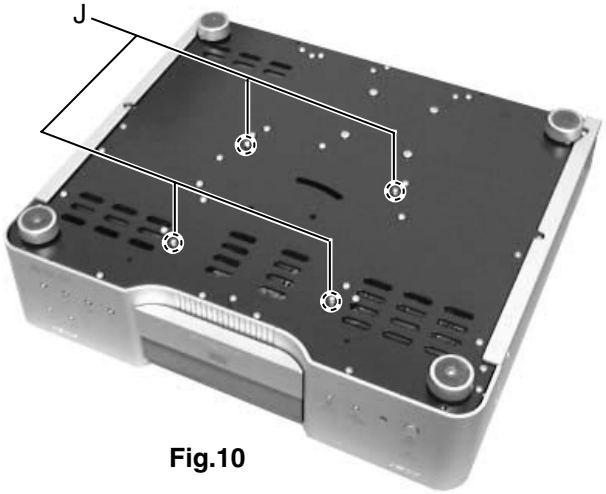


Fig.10

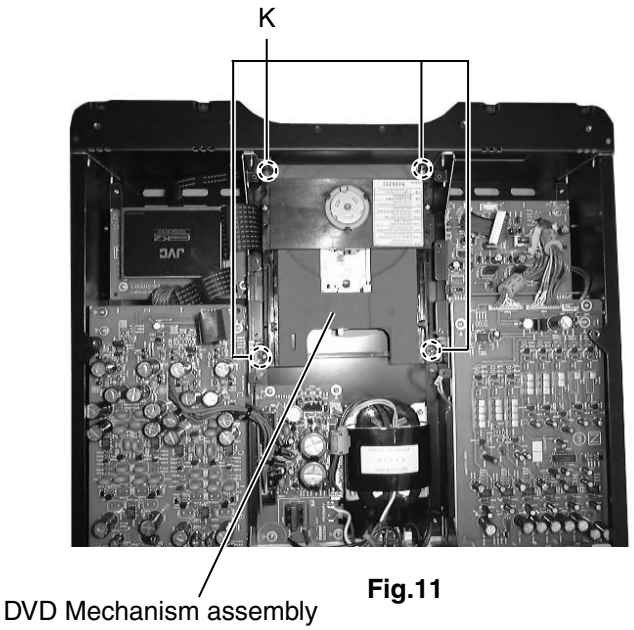


Fig.11

■ Removing the audio(rear L/R) board (See Fig.12~13)

*Prior to performing the following procedure, remove the top panel.

1.Remove the two screws **L** attaching the audio(rear L/R) board.

2.Remove the four screws **M** attaching the audio(rear L/R) board from back of the body.

3.Disconnect the card wire from CN761 on the audio(rear L/R) board.

4.Disconnect the connector from CN697 on the audio power board.

5.Solder on the audio (rear L/R) board is removed and disconnect the earth wire from W7901.

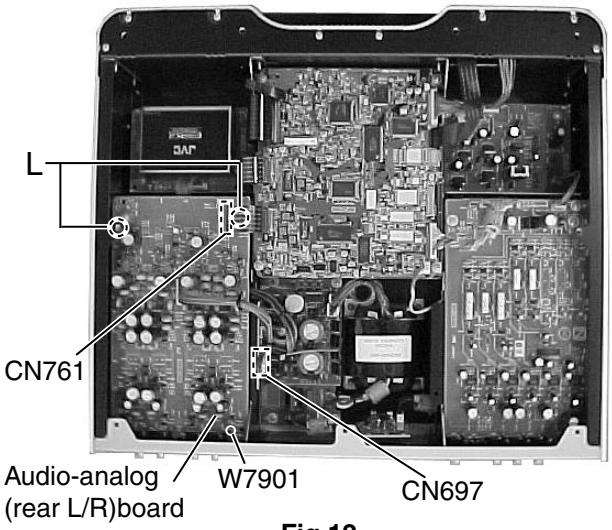


Fig.12

Fig.13

■ Removing the audio(front L/R) board (See Fig.14)

*Prior to performing the following procedure, remove the top panel.

1.Remove the audio(rear L/R) board(upper step).

2.Remove the two screws **N** of the pillar which supports audio(rear L/R) board(upper step).

3.Remove the two screws **O** attaching the audio(front L/R)board.

4.Disconnect the connector from CN721 and CN722 on the audio signal(front) output terminal.

5.Disconnect the connector from CN695 and CN696 on the DVD audio power board.

6.Disconnect the connector from CN741 on the signal processing board.

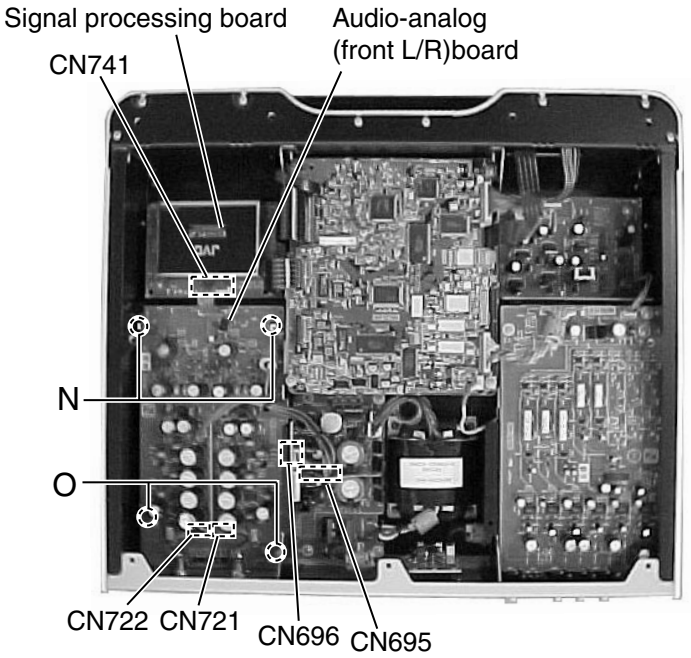


Fig.14

■ Removing the video signal board(See Fig.15,16)

*Prior to performing the following procedure, remove the top panel.

1.Remove the three screws **P** attaching the video signal board.

2.Remove the five screws **Q** attaching the video signal board from back of the body.

3.Disconnect the connector from CN502 on the main board.

4.Disconnect the connector from CN601 on the video signal board.

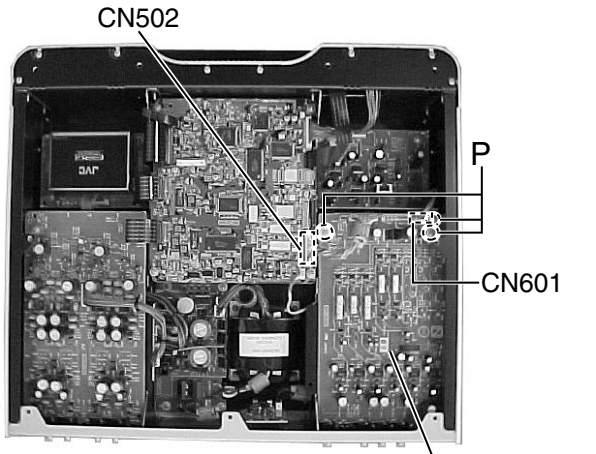


Fig.15

■ Removing the power supply board (See Fig.17,18)

*Prior to performing the following procedure, remove the top panel, rear cover and video signal board.

1.Remove the two screws **S** attaching the power supply board cover.

2.Remove the four screws **T** attaching the power supply board cover and it is remove.

3.Remove the two screws **U** of the pillar which supports power supply board cover.

4.Remove the four screws **V** and two screws **V'** attaching the power supply board.

5.Disconnect the connector from CN991 on the power supply board.

6.Disconnect the connector from CN501 and CN506 on the main board.

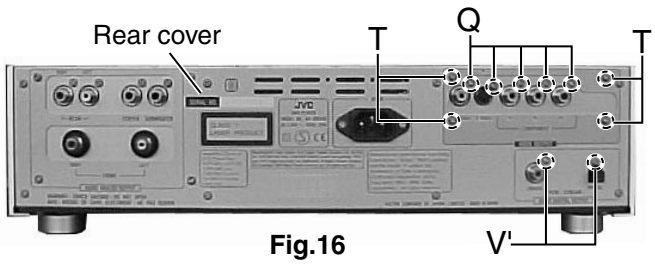


Fig.16

Fig.17

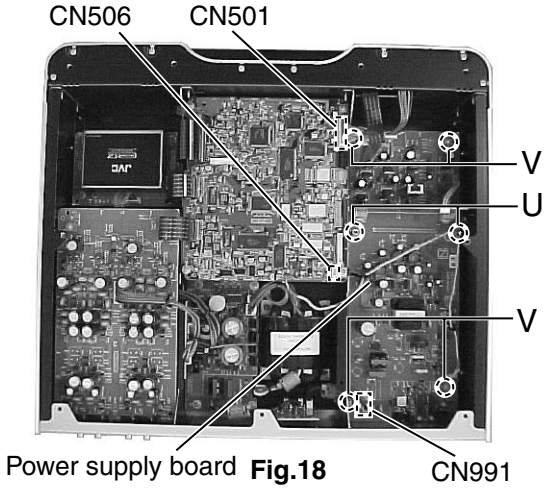


Fig.18

■ Removing the signal processing board (See Fig.19)

*Prior to performing the following procedure, remove the top panel.

1.Remove the four screws **W** attaching the signal processing board.

2.Disconnect the connector from CN711 and CN741 on the signal processing board.

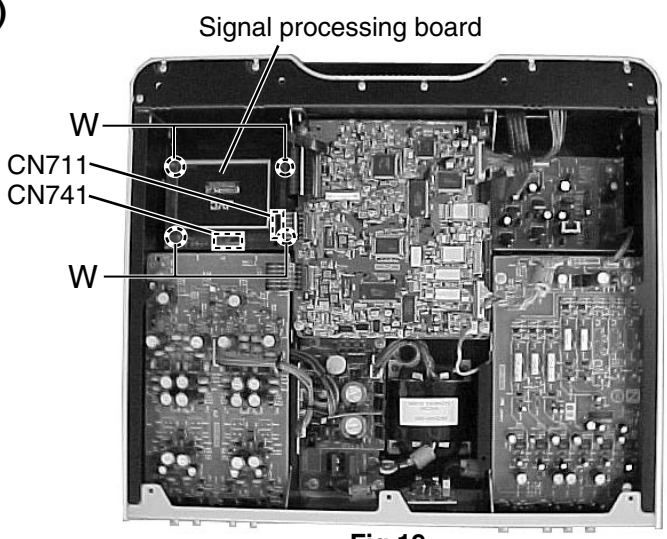


Fig.19

■ Removing the audio-power supply board (See Fig.20)

*Prior to performing the following procedure, remove the top panel and rear cover.

1.Remove the four screws **X** attaching the audio-power supply board.

2.Disconnect the connector from CN691,CN692,CN695, CN696,CN697 on the audio-power supply board.

3.The solder(PP691 and PP692) of wire connected with power transformer is removed.

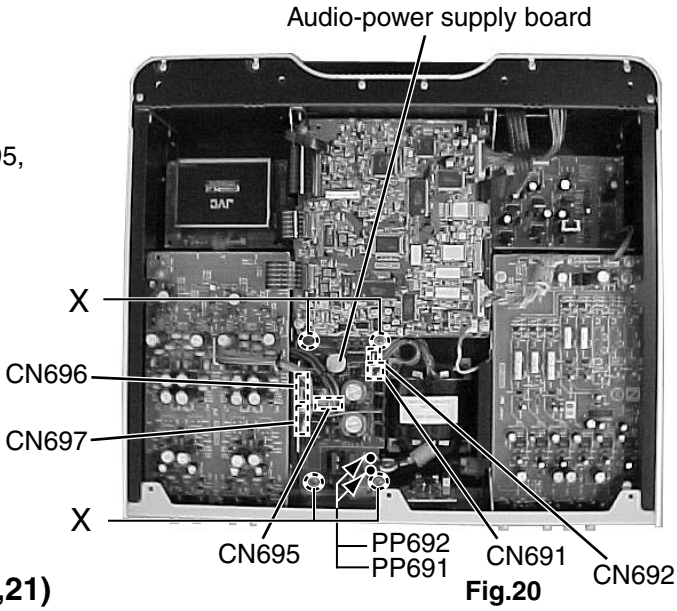


Fig.20

■ Removing the power transformer (See Fig.20,21)

*Prior to performing the following procedure, remove the top panel.

1.Disconnect the connector from CN691 and CN692 on the audio-power supply board.

2.The solder(PP691 and PP692) of wire connected with power transformer is removed.

3.Remove the four screws **Y** attaching the power transformer from bottom of the body.

<ATTENTION>
Please the power transformer must become unstable and put up the main body sideways, and work while supporting the power transformer by one of hands when you remove the screw of the power transformer.

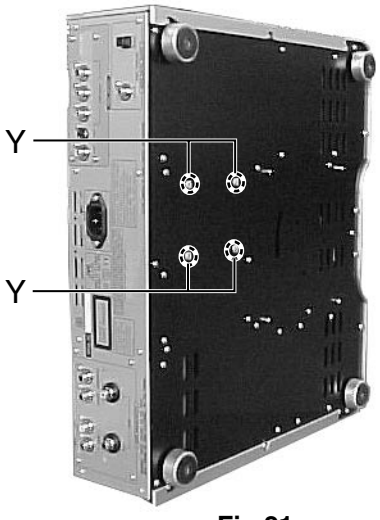


Fig.21

■ Removing the operation switch board/ FL and operation switch board(See Fig.22)

1.Remove the front panel assembly.(See Fig.1~5)

2.Remove the ten screws **Z** attaching the FL and operation switch board.

3.Remove the seven screws **Z'** attaching the operation switch board.

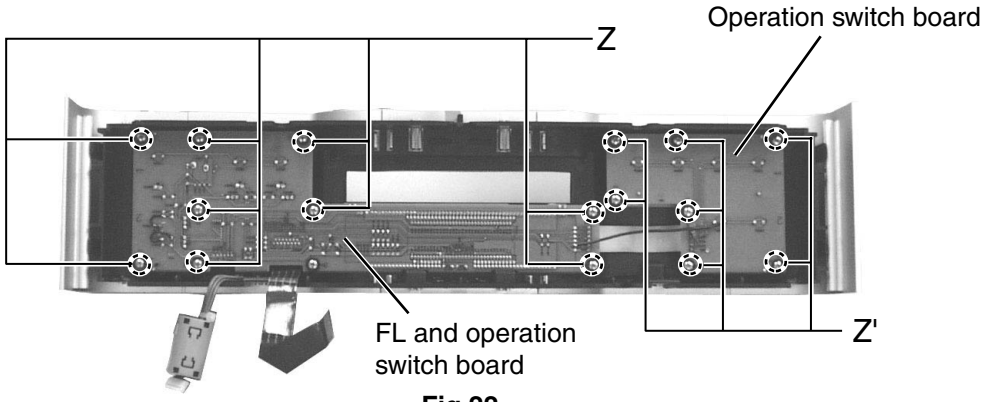


Fig.22

<Removing DVD mechanism unit>

■ **Removing the clamper base** (See Fig.1)

* Remove the top cover.
* Remove the DVD mechanism unit.

1. Remove the two screws **A** attaching the clamper base.

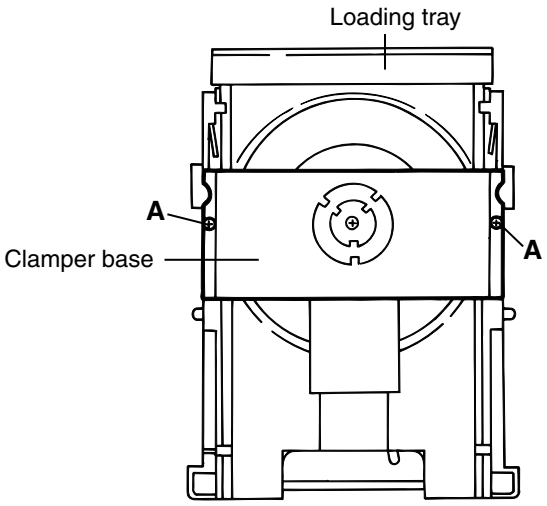


Fig.1

■ **Removing the loading tray** (See Fig.2~4)

* Remove the clamper base.

1. Turn the up-down cam lever clockwise (in the direction of the arrow in Fig.2) to lower the position of the mechanism.
2. Manually set the loading tray to the fully-open position.
3. Stretch the tray stoppers on both sides of the loading base outward and pull out the tray.

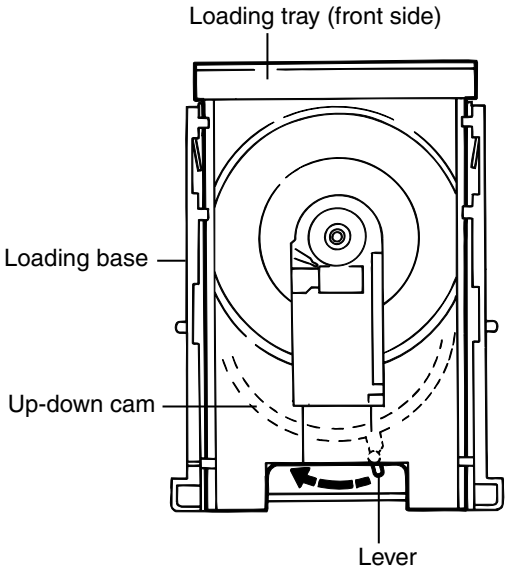


Fig.2

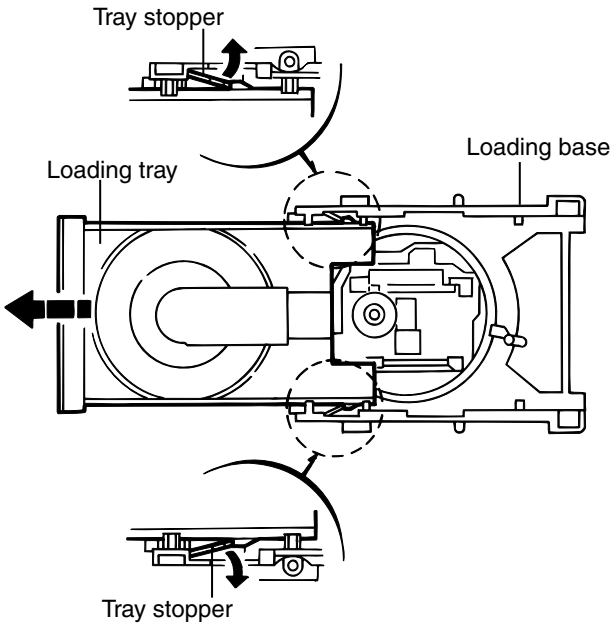


Fig.4

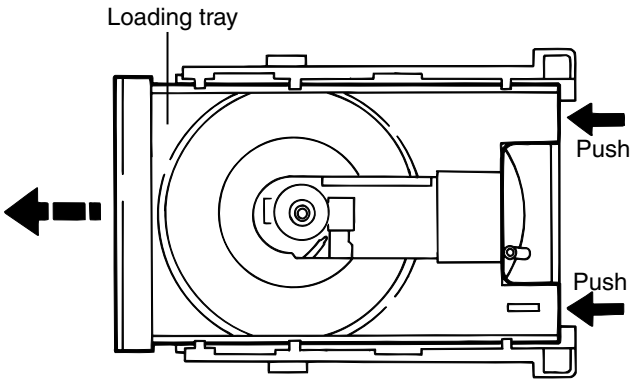


Fig.3

■**Removing the traverse mechanism unit** (See Fig.5)

* Remove the loading tray.

1. Remove the three screws **B** attaching the traverse mechanism unit.

■**Protecting the optical pickup**

* Solder the flexible ground point on the optical pickup when replacing the pickup or before detaching the mechanism control board. When assembling the unit, remove the solder last.

■**Removing the mechanism control board** (See Fig.6~7)

* Remove the traverse unit. (Can be detached without detaching the T-mechanism unit.)

1. Remove the two screws **C** attaching the mechanism control base from the bottom of the traverse unit.
2. Pull out the CN12 connector and detach the mechanism control board.
3. Remove the card wire from the CN13 connector on the mechanism control board.
4. Pull out the FPC holder from the CN12 connector on the reverse side of the mechanism control board and remove the flexible harness, referring to Fig.7.

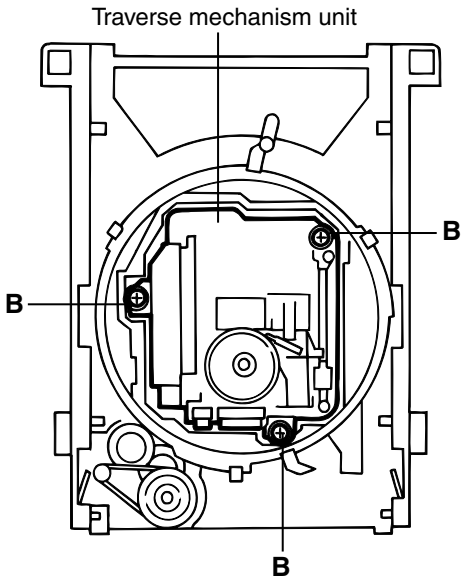


Fig.5

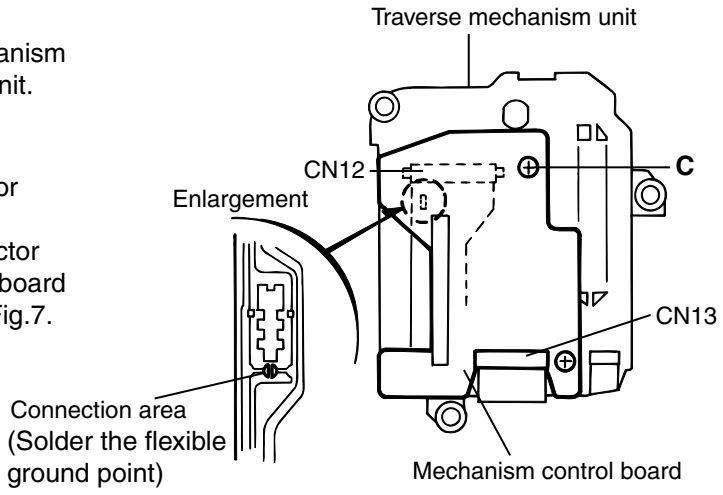


Fig.6

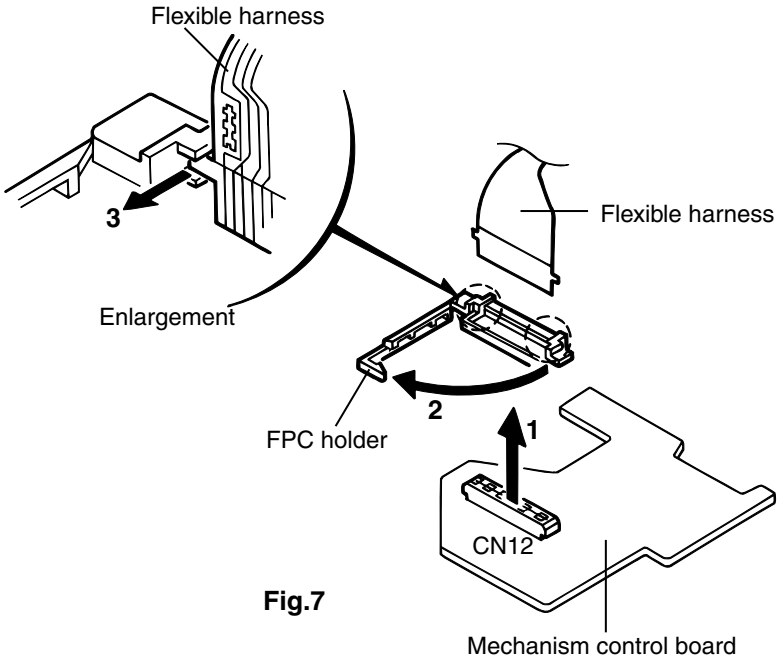


Fig.7

■ **Removing the turntable and spindle motor assembly** (See Fig.8~9)

* Remove the traverse mechanism unit.
* Solder the flexible ground point on the optical pickup. (See Fig.6)
* Remove the mechanism control board.

1. Remove the flexible harness from the feed motor connector on the spindle motor board assembly.
2. Remove the three screws **D** attaching the spindle motor from the bottom of the traverse chassis.

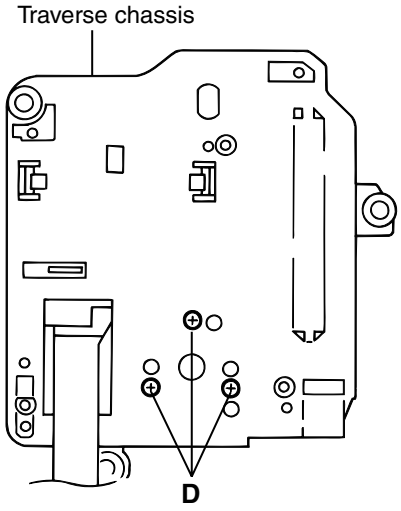


Fig.8

■ **Removing the feed motor unit** (See Fig.9)

* Remove the traverse mechanism unit.
* Remove the mechanism control board.

1. Remove the FPC from the feed motor connector on the turntable spindle motor board.
2. Remove the two screws **E** attaching the feed motor unit.

■ **Removing the optical pickup unit** (See Fig.9)

* Remove the traverse mechanism unit.
* Remove the mechanism control board.
* Remove the feed motor unit.

1. Remove the screw **F** attaching the guide shaft holder at **b**, then simultaneously remove the guide shaft at B and the optical pickup unit. While doing so, slide the unit horizontally away from the guide shaft at **a**.

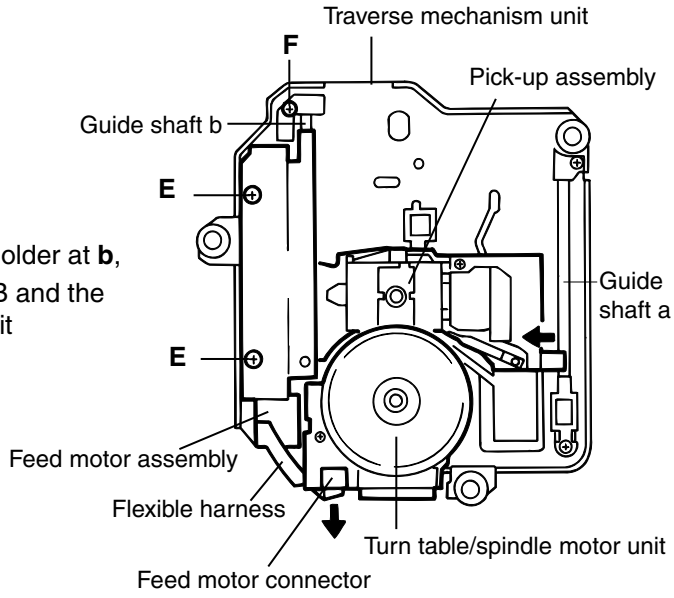


Fig.9

■ Removing **the loading mechanism parts** (See Fig.10~11)

* Remove the clamper base.

* Remove the disk tray.

1. Turn the lever counterclockwise until it stops (position 1), while pushing the switch lever in the direction of the arrow and pushing up the pawl at **a** using a screwdriver.
2. Stretch the two pawls at **b** outward using a screwdriver and remove the chassis.
3. Turn the lever clockwise (position 2) to remove the up-down cam.
4. Remove the pulley gear and the pulley gear belt after removing the screw **G** attaching the pulley gear.
5. Pull out drive gear 2 then drive gear 1.

■ **Removing the loading motor board** (See Fig.11~12)

* Remove the clamper base.

* Remove the disk tray.

1. Remove the loading belt.
2. Remove the two screws **H** attaching the loading motor.
3. Remove the screw at **I** and the three pawls at **c** fixing the loading motor base from the reverse side of the loading base.

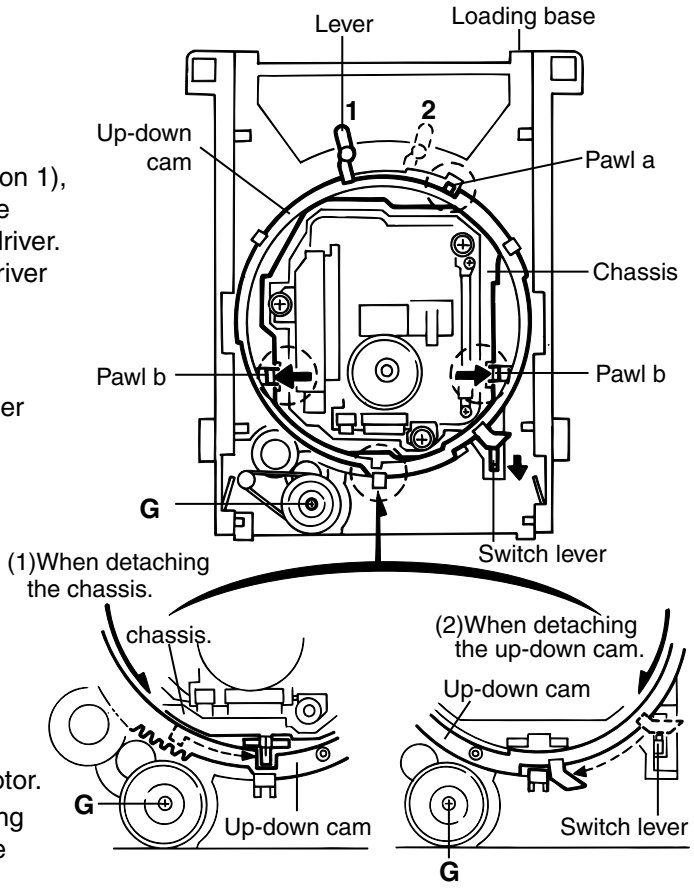


Fig.10

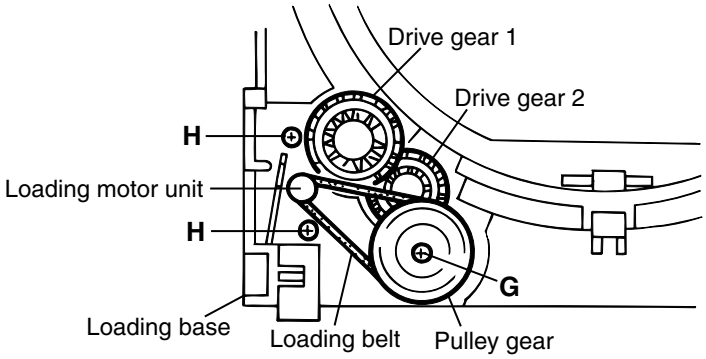


Fig.11

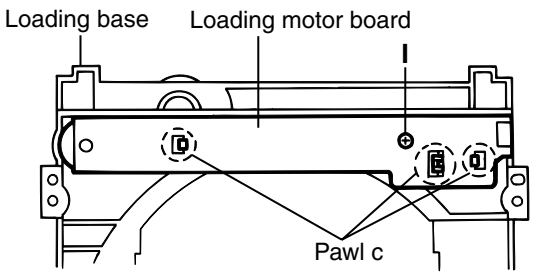


Fig.12

Method of initializing EEPROM and display of jitter value

■ Initializing EEPROM

Please initialize EEPROM when you exchange Microcomputer(IC401,IC402) and optical pick-up by the undermentioned method.

1. It is confirmed that there is no disk in the tray.

2. The power supply plug is inserted while pushing the PLAY key and the OPEN/CLOSE key to the main body.

3. It is displayed in the FL display part as "TEST E2".

4. The EX K2 key is pushed of the main body.

5. The POWER key is pushed if displayed in the FL display part as "EEP_****".
   (**** is a check sum of device key display.)

6.When normally entering the state of the power standby, initialization is normal and completion.

■ Jitter value (We will separately inform of the method of adjusting jitter.)

1. It is confirmed that there is no disk in the tray.

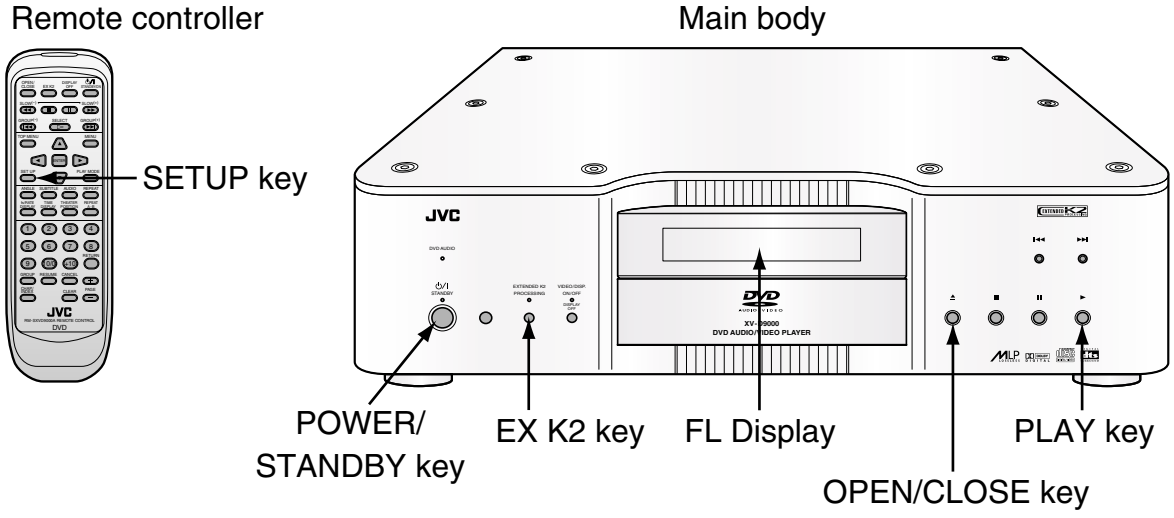
2. The power supply plug is inserted while pushing the PLAY key and the OPEN/CLOSE key to the main body.

3. It is displayed in the FL display part as "TEST E2".

4. Press the OPEN/CLOSE key to move the tray outward.
   Put the test disc (VT-501) on the tray and press OPEN/CLOSE key.
   The tray should move inward (NOTE:Don't push to close the tray directly by hand etc,)

5.Keeps pushing SETUP key to remote controller for ten seconds or more.

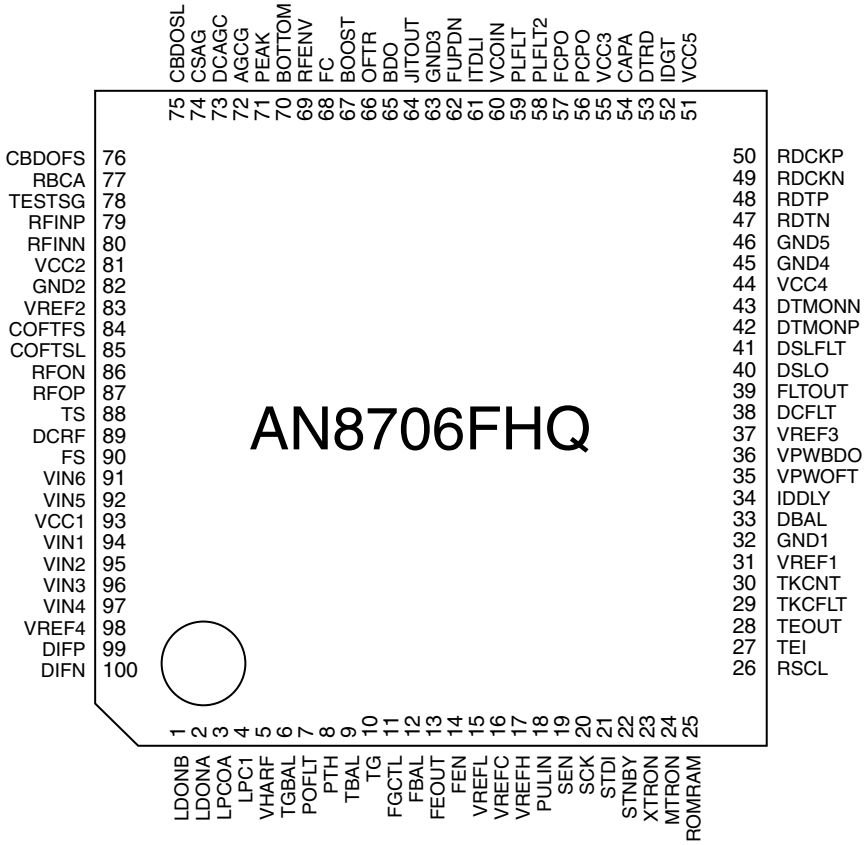
6.Press the PLAY key of the main body.



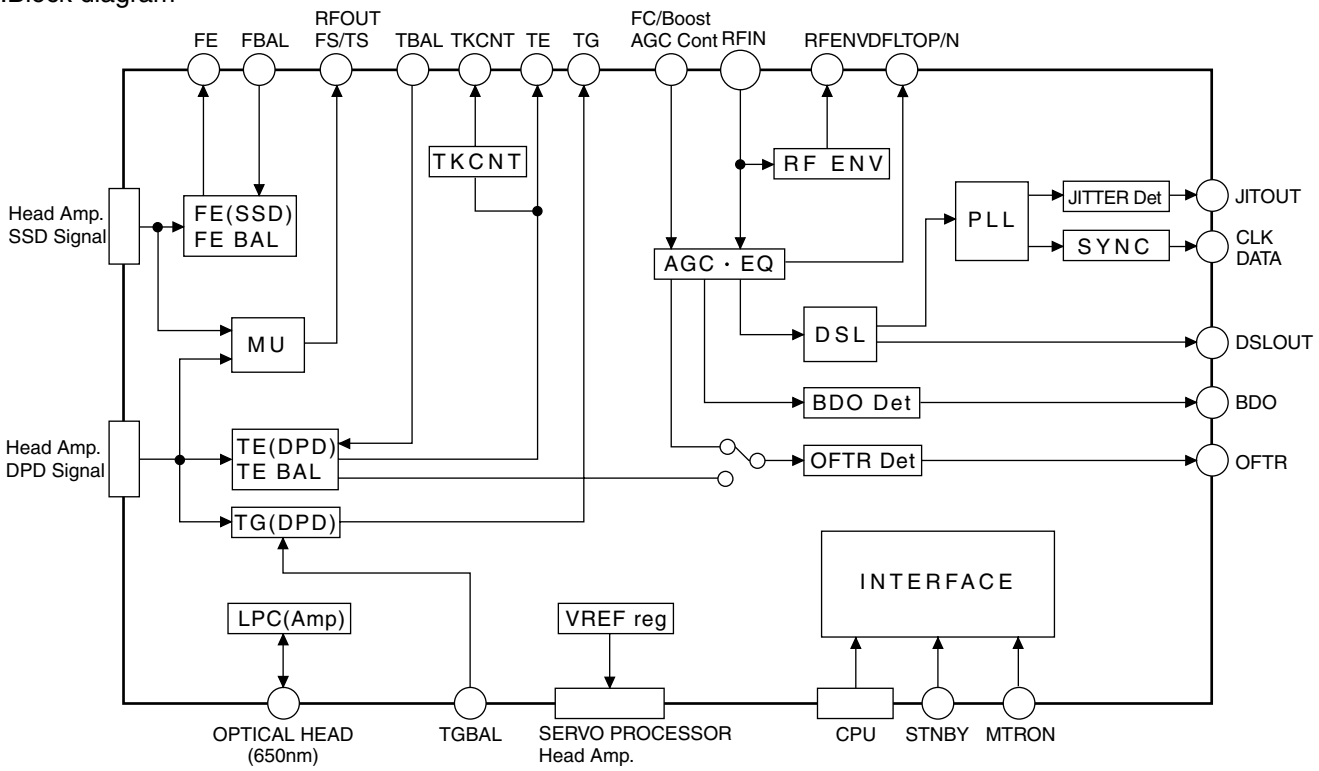
Description of major ICs

■ AN8706FHQ (IC101) : Front end processor

1.Pin layout



2.Block diagram



3.Pin function

AN8706FHQ (1/2)

Pin No.	Symbol	I/O	Functions
1	LDONB	I	Laser ON (CD Head) terminal
2	LDONA	I	Laser ON (DVD Head) terminal
3	LPCOA	O	Laser drive output terminal
4	LPC1	I	Laser PIN input terminal
5	VHARF	O	VHALF voltage output terminal
6	TGBAL	I	Tangential phase balance control terminal
7	POFLT	O	Track detection Threshold value level terminal
8	PTH	I	Track detection Threshold value level terminal
9	TBAL	I	Tracking balance control terminal
10	TG	O	Tangential phase error signal output terminal
11	FGCTL	I	Focus amplifier Gain control terminal
12	FBAL	I	Focus balance control terminal
13	FEOUT	O	Focus error signal output terminal
14	FEN	I	Focus error output amplifier reversing input terminal
15	VREFL	O	VREFL voltage output terminal
16	VREFC	O	VREFC voltage output terminal
17	VREFH	O	VREFH voltage output terminal
18	PULIN	I	DSL,PLL drawing mode switch terminal
19	SEN	I	SEN(Cereal data input terminal)
20	SCK	I	SCK(Cereal data input terminal)
21	STDI	I	STDI(Cereal data input terminal)
22	STNBY	I	Standby mode control terminal
23	XTRON	I	Tracking OFF holding input terminal
24	MTRON	I	Monitor output ON/OFF switch terminal
25	ROMRAM	I	ROM･RAM switch terminal
26	RSCL	O	Standard current source terminal
27	TEI	I	Tracking error output Amp reversing input terminal
28	TEOUT	O	Tracking error signal output terminal
29	TKCFLT	O	Track count detection filter terminal
30	TKCNT	O	Track count output terminal
31	VREF1	O	VREF1 voltage output terminal
32	GND1	O	Earth terminal 1
33	DBAL	I	Data slice offset adjustment terminal
34	IDDLY	I	Data slice delay adjustment terminal
35	VPWOFT	I	OFTR detection level setting terminal
36	VPWBDO	I	BDO detection level setting terminal
37	VREF3	O	VREF3 voltage output terminal
38	DCFLT	O	Capacity connection terminal for data slice input filter
39	FLTOUT	O	Filter amplifier output terminal
40	DSLO	O	Data slice single data output terminal
41	DSLFLT	O	Constant filter terminal when data is sliceddelly
42	DTMONP	O	PLL differential motion 2 making to value edge signal monitor output (+)
43	DTMONN	O	PLL differential motion 2 making to value edge signal monitor output (-)
44	VCC4	I	Power terminal 4 (5V)
45	GND4	O	Earth terminal 4
46	GND5	O	Earth terminal 5
47	RDTN	O	PLL differential motion making to synchronization RF signal reversing output
48	RDTP	O	PLL differential motion making to synchronization RF signal rotation output
49	RDCKN	O	PLL differential motion making synchronization clock reversing output
50	RDCKP	O	PLL differential motion making synchronization clock rotation output

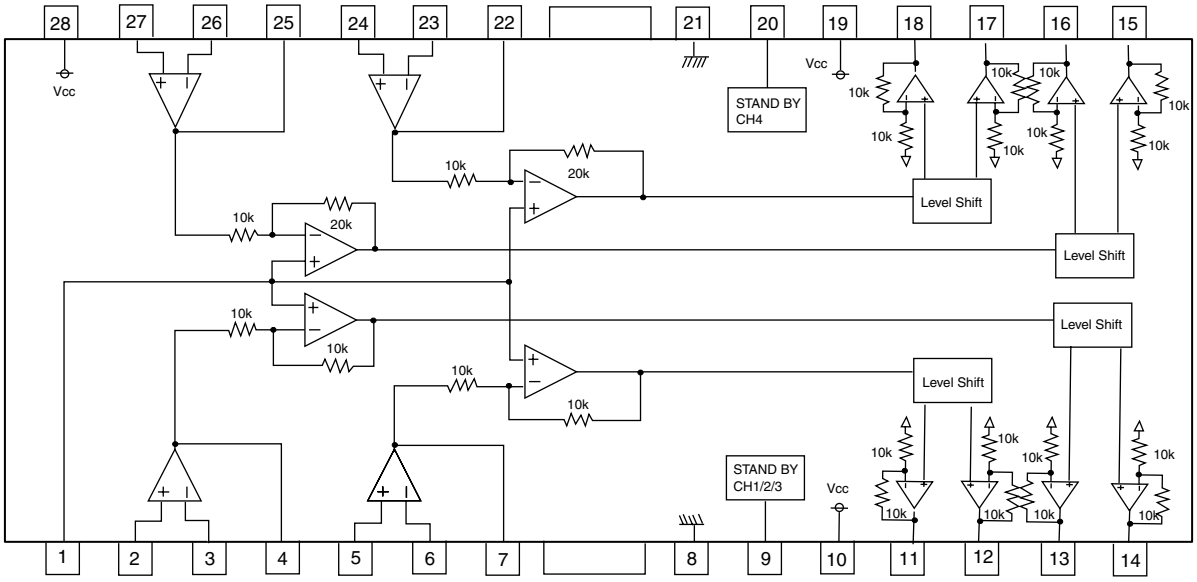
3.Pin function

AN8706FHQ(2/2)

Pin No.	Symbol	I/O	Functions
51	VCC5	I	Power terminal 5 (3.3V)
52	IDGT	I	Data slice part address part gate signal input terminal (For RAM)
53	DTRD	I	Data slice data read signal input terminal(For RAM)
54	CAPA	I	Data slice CAPA(Address)signal input terminal (For RAM)
55	VCC3	I	Power terminal 3 (5V)
56	PCPO	O	PLL phase gain set terminal
57	FCPO	O	PLL frequency gain set terminal
58	PLFLT2	O	PLL low region filter terminal
59	PLFLT	O	PLL high region filter terminal
60	VCOIN	I	PLL VCO input terminal
61	ITDLI	O	PLL jitter free current ripple removal filter terminal
62	FUPDN	I	PLL frequency control input terminal
63	GND3	O	Earth terminal 3
64	JITOUT	O	Detection signal output of jitter
65	BDO	O	BDO output terminal
66	OFTR	O	OFTR output terminal
67	BOOST	I	Booth control terminal for filter
68	FC	I	FC control terminal for filter
69	RFENV	O	RF envelope output terminal
70	BOTTOM	O	Bottom envelope detection filter terminal
71	PEAK	O	Peak envelope detection filter terminal
72	AGCG	O	AGC amplifier gain control terminal
73	DCAGC	O	AGC amp filter terminal
74	CSAG	O	Sag cancellation circuit filter terminal
75	CBDOSL	O	BDO detection capacitor terminal
76	CBDOFS	O	BDO detection capacitor terminal
77	RBCA	O	BCA detection level setting terminal
78	TESTSG	I	TEST signal input terminal
79	RFINP	I	RF signal positive moving input terminal
80	RFINN	I	RF signal reversing input terminal
81	VCC2	I	Power terminal 2 (5V)
82	GND2	O	Earth terminal 2
83	VREF2	O	VREF2 voltage output terminal
84	COFTFS	O	OFTR detection capacitor terminal
85	COFTFL	O	OFTR detection capacitor terminal
86	RFON	O	RF signal output terminal P
87	RFOP	O	RF signal output terminal N
88	TS	O	All addition amplifier (DVD) output terminal
89	DCRF	O	All addition amplifier capacitor terminal
90	FS	O	All addition amplifier (CD) output terminal
91	VIN6	I	Focus input of external division into two terminal
92	VIN5	I	Focus input of external division into two terminal
93	VCC1	I	Power terminal 1 (5V)
94	VIN1	I	External division into four (DVD/CD) RF input terminal 1
95	VIN2	I	External division into four (DVD/CD) RF input terminal 2
96	VIN3	I	External division into four (DVD/CD) RF input terminal 3
97	VIN4	I	External division into four (DVD/CD) RF input terminal 4
98	VREF4	O	VREF4 voltage output terminal
99	DIFP	O	RF signal (RAM) output terminal P
100	DIFN	O	RF signal (RAM) output terminal N

■ BA5983FM-X (IC271) : 4CH DRIVER

1.Block diagram

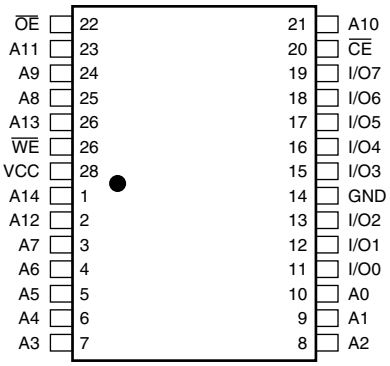


2.Pin function

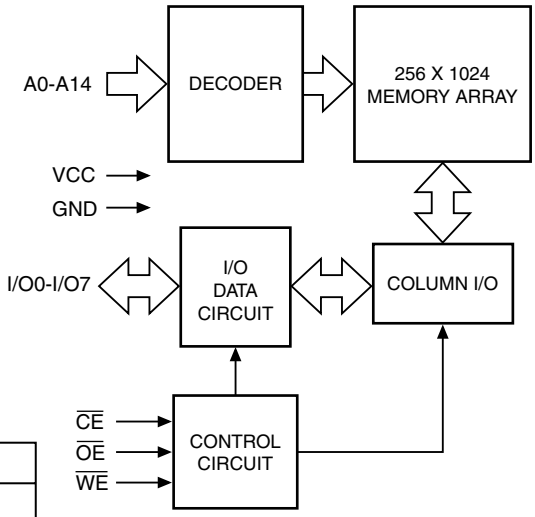
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	BIAS IN	I	Input for Bias-amplifier	15	VO4(+)	O	Non inverted output of CH4
2	OPIN1(+)	I	Non inverting input for CH1 OP-AMP	16	VO4(-)	O	Inverted output of CH4
3	OPIN1(-)	I	Inverting input for CH1 OP-AMP	17	VO3(+)	O	Non inverted output of CH3
4	OPOUT1	O	Output for CH1 OP-AMP	18	VO3(-)	O	Inverted output of CH3
5	OPIN2(+)	I	Non inverting input for CH2 OP-AMP	19	PowVcc2	-	Vcc for CH3/4 power block
6	OPIN2(-)	I	Inverting input for CH2 OP-AMP	20	STBY2	I	Input for Ch4 stand by control
7	OPOUT2	O	Output for CH2 OP-AMP	21	GND	-	Substrate ground
8	GND	-	Substrate ground	22	OPOUT3	O	Output for CH3 OP-AMP
9	STBY1	I	Input for CH1/2/3 stand by control	23	OPIN3(-)	I	Inverting input for CH3 OP-AMP
10	PowVcc1	-	Vcc for CH1/2 power block	24	OPIN3(+)	I	Non inverting input for CH3 OP-AMP
11	VO2(-)	O	Inverted output of CH2	25	OPOUT4	O	Output for CH4 OP-AMP
12	VO2(+)	O	Non inverted output of CH2	26	OPIN4(-)	I	Inverting input for CH4 OP-AMP
13	VO1(-)	O	Inverted output of CH1	27	OPIN4(+)	I	Non inverting input for CH4 OP-AMP
14	VO1(+)	O	Non inverted output of CH1	28	PreVcc	-	Vcc for pre block

■ IS61LV256-12T(IC163,IC164,IC165,IC173):32k X 8 Low voltage CMOS Static RAM

1.Pin layout



2.Block diagram



3.Pin function

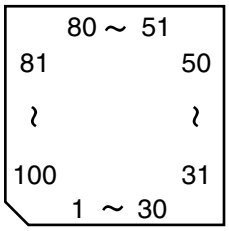
Pin No.	Symbol	I/O	Function
1	A14	I	Address input
2	A12	I	Address input
3~10	A7~A0	I	Address input
11~13	I/O0~I/O2	I/O	Data I/O
14	GND	-	Connects with the ground
15~19	I/O3~I/O7	I/O	Data I/O
20	$\overline{CE}$	I	Chip enable input
21	A10	I	Address input
22	$\overline{OE}$	I	Output enable input
23	A11	I	Address input
24,25	A9,A8	I	Address input
26	A13	I	Address input
27	$\overline{WE}$	I	Write enable input
28	VCC	-	Power supply terminal

■ JCE8011(IC551):Graphic controller

Pin No.	Symbol	I/O	Function
1~8	VD0~7	I	DVD Image signal input (Multi plex data Y,Cr,Cb)
9	VCLKI	I	Dot clock signal input (27MHz)
10	HSYNCI	I	The horizontal synchronous signal input
11	VSYNCI	I	Vertical synchronous signal input
12	VCC	-	Power supply
13	VCLKO	O	Dot clock signal output (27MHz)
14	HSYNCO	O	'H' blanking output
15	VSYNCO	O	'V' blanking output
16~23	DOUT0~7	O	Digital data output
24	TEST	-	Test terminal (Uses as GND usually)
25	RESETB	I	System reset signal
26	GND	-	Connect to GND
27	NTB	I	Mode switching NTSC(low) / PAL(high)
28	DTSF0	I	Taking timing shift of VD input
29	DTSF1	I	Taking timing shift of VD input
30	VIDEG	I	Taking edge specification of VD input (0:up , 1:down)
31	DOSF0	I	Timing shift input of output data
32	DOSF1	I	Timing shift input of output data
33	XVRST	O	Non connect
34	F1	O	Field Identification signal output
35	HBL	O	'H' blanking output
36	VBL	O	'V' blanking output
37	VOEDG	I	Output timing setting of DOUT (0:up , 1:down)
38	VCC	-	Power supply
39~46	FRD7~0	I	Field memory read data input
47	GND	-	Connect to GND
48	FRCK	O	Field memory read clock
49	FWCK	O	Field memory write clock
50	FREB	O	Field memory read enable
51	FWEB	O	Field memory write enable
52	FRRSTB	O	Field memory read address reset
53	FWRSTB	O	Field memory write address reset
54~61	FWD7~0	O	Field memory write data output
62	VCC	-	Power supply
63~70	CHD7~0	I	Character ROM data
71	GND	-	Connect to GND
72	CHOEB	O	Character ROM output enable
73~82	CHA19~10	O	Character ROM address output
83	VCC	-	Power supply
84~93	CHA9~0	O	Character ROM address output
94	GND	-	Connect to GND
95	ACK	O	
96	CS1B	I	Serial data chip select for graphic control
97	CS2B	I	Serial data chip select for encoder control
98	SCK	I	Serial clock input
99	RXD	I	Serial input data
100	TXD	O	Serial output data

■ JCV8005-2(IC471):CPPM

1.Pin layout



2.Pin function

JCV8005-2 1/2

Pin No.	Symbol	I/O	Description
1	VDD	-	Power supply
2	GND	-	Connect to ground
3~10	HDATA0~7	I/O	Data input/output terminal (both by 8 bits)
11	VDD	-	Power supply
12	GND	-	Connect to ground
13~20	HADDR0~7	I	8 bit address bus to internal address (connect to host)
21	VDD	-	Power supply
22	GND	-	Connect to ground
23	NCS	I	Chip select signal from host
24	NRD	I	Data read signal from host
25	NWR	I	Data write signal from host
26	NIRQ	O	Interrupt of request to host
27	WAIT	O	Wait demand to host
28	NRESET	I	Reset signal from host
29	VDD	-	Power supply
30	GND	-	Connect to ground
31	VDD	-	Power supply
32	GND	-	Connect to ground
33~36	STD7~4_OUT	O	Data output to DVD decoder (8 bits)
37	GND	-	Connect to ground
38~41	STD3~0_OUT	O	Data output to DVD decoder (8 bits)
42	VDD	-	Power supply
43	GND	-	Connect to ground
44	REQ_IN	I	Request signal for forwarding control by decoder
45	DACK_OUT	O	Output signal to decoder which shows effective data
46	STCLK_OUT	O	Data strobe signal to decoder
47	SYNC_OUT	O	Sector sink signal to decoder
48	STERROUT	-	Non connect
49	VDD	-	Power supply
50	GND	-	Connect to ground
51	VDD	-	Power supply
52	GND	-	Connect to ground
53	NG_RD	I	Glue logic input signal from host
54	NG_WR	I	Glue logic input signal from host
55	G_WITODC	I	Glue logic input signal from front end
56	G_CSDEC	I	Glue logic input signal from host
57	G_WITDEC	I	Glue logic input signal from decoder
58	VDD	-	Power supply

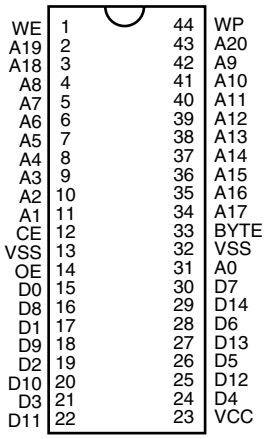
2.Pin function

JCV8005-2 2/2

Pin No.	Symbol	I/O	Description
59	GND	-	Connect to ground
60	WAIT1	O	Glue logic output signal to host
61	WAIT2	-	Non connect
62	WAITIN	I	Glue logic input signal (connect to 27 pin)
63	VDD	-	Power supply
64	GND	-	Connect to ground
65	TEST_IN	I	Connect to ground
66,67	NC	-	Non connect
68	VDD	-	Power supply
69	GND	-	Connect to ground
70	CLKOCTL	I	Input terminal for crystal-oscillator circuit on/off control
71	NC	-	Non connect
72	OSCI	I	Crystal oscillation terminal (input side)
73	OSCO	O	Crystal oscillation terminal (output side)
74	NC	-	Non connect
75	VDD	-	Power supply
76	GND	-	Connect to ground
77	33OUT	O	Oscillation output terminal
78	16OUT	O	Oscillation output terminal
79	VDD	-	Power supply
80	GND	-	Connect to ground
81	VDD	-	Power supply
82	GND	-	Connect to ground
83	STERR_IN	I	Presence of data error from front end
84	SYNC_IN	I	Sector sink signal from front end
85	STCLK_IN	I	Data clock signal from front end
86	DACK_IN	I	Signal which shows effective data from front end
87	REQ_OUT	O	Request signal for forwarding control to front end
88	VDD	-	Power supply
89	GND	-	Connect to ground
90~93	STD0~3_IN	I	Data input from front end (8 bits)
94	GND	-	Connect to ground
95~98	STD4~7_IN	I	Data input from front end (8 bits)
99	VDD	-	Power supply
100	GND	-	Connect to ground

■ M27C1602CZ(IC402,IC553):16M ROM

1.Pin layout

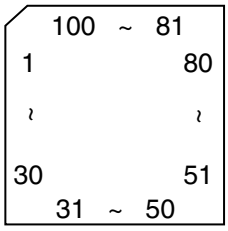


2.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WE	I	Write enable	23	VCC	-	Power supply +3.3V
2	A19	I	Address bus 19	24	D4	O	Data bus 4
3	A18	I	Address bus 18	25	D12	O	Data bus 12
4	A8	I	Address bus 8	26	D5	O	Data bus 5
5	A7	I	Address bus 7	27	D13	O	Data bus 13
6	A6	I	Address bus 6	28	D6	O	Data bus 6
7	A5	I	Address bus 5	29	D14	O	Data bus 14
8	A4	I	Address bus 4	30	D7	O	Data bus 7
9	A3	I	Address bus 3	31	A0	I	Address bus 0
10	A2	I	Address bus 2	32	VSS	-	Connect to GND
11	A1	I	Address bus 1	33	BYTE	I	Data width selection input
12	CE	I	Chip enable	34	A17	I	Address bus 17
13	VSS	-	Connect to GND	35	A16	I	Address bus 16
14	OE	I	Output enable	36	A15	I	Address bus 15
15	D0	O	Data bus 0	37	A14	I	Address bus 14
16	D8	O	Data bus 8	38	A13	I	Address bus 13
17	D1	O	Data bus 1	39	A12	I	Address bus 12
18	D9	O	Data bus 9	40	A11	I	Address bus 11
19	D2	O	Data bus 2	41	A10	I	Address bus 10
20	D10	O	Data bus 10	42	A9	I	Address bus 9
21	D3	O	Data bus 3	43	A20	I	Address bus 20
22	D11	O	Data bus 11	44	WP	-	Non connect

■ M30622EC-FP(IC451):System controller

1.Pin layout



2.Key Matrix

	KEY IN 0	KEY IN 1	KEY IN 2
KEY OUT 0	POWER	K2	DISPLAY OFF
KEY OUT 1	OPEN/CLOSE	STOP	PAUSE
KEY OUT 2	⏮	⏭	PLAY

3.Pin Function (1/2)

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	FLDAT	O	FL driver data output	34	CPURST	O	CPU Reset signal output
2	FLSCK	O	FL driver clock output	35	S2UDT	O	Communication data output
3	CS4	O	VFPIC chip select output				for unit micon
4	VLINEOFF	O	Video line OFF control	36	U2SDT	I	Communication data input
5	EEPEI	I	EEPROM set data input				From unit micon
6	EEPEO	O	EEPROM set data output	37	SCLK	I	System clock signal input
7	EECK	O	EEPROM clock signal output	38	DSPRST	O	Reset signal output for DSP
8	GND	-	Connect to ground	39	BANK	O	OSDROM switch output
9	GND	-	Connect to ground	40	ACK	I	OSD active input
10	EECS	O	EEPROM chip select	41	TRAYOUT	O	Tray open detection signal
11	POWERON	O	Power on signal output	42	OSDCS1	O	OSD Chip select
12	RESET	I	Reset signal input	43	OSDCS3	O	Encoder Chip select
13	XOUT	O	Clock signal output	44	ENCDRST	O	Encoder reset
14	VSS	-	Connect to ground	45	K2RESET	O	K2 Reset signal output
15	XIN	I	Clock signal input	46	VS1	O	S1 Switch output
16	VCC	-	Power supply +5V	47	VCD	O	Video mode switch output
17	NMI	-	Non connect	48	MULTI/2CH	-	Non connect
18	REQ	I	Request signal input	49	96K/48K	-	Non connect
19	REMO	I	Remote control signal input	50	DDCLK	O	Clock signal output for DAC
20	VSYNC	I	Video sync input	51	DDDATA	O	Data output for DAC
21	TRAYIN	I	Tray close detection signal	52	DDCS1	O	Chip select output for front CH
22	BUSY	O	Busy signal output	53	DDCS2	O	Chip select output for rear CH
23	SS1	O	Selection output for DSP1	54	K2ONOFF	O	K2 power control output
24	SS2	O	Selection output for DSP2	55	192K/48K	O	Switch output of front CH lpffc
25	HREQ1	I	Request signal input for DSP1	56	GAINSL	O	Gain switch output of rear Lch
26	HREQ2	I	Request signal input for DSP2	57	GAINSR	O	Gain switch output of rear Rch
27	OSDCS2	O	OSD Chip select signal	58	GAINNC	O	Gain switch output of center CH
28	OSDCK	O	OSD Clock signal	59	GAINLFE	O	Gain switch output of LFE CH
29	OSDDI	I	OSD Data input	60	MLPSEL2	O	Master clock switch output of DSP
30	OSDDO	O	OSD Data output	61	MLPSEL1	O	Master clock switch output of DSP
31	MDSPOUT	O	Data output for DSP	62	VCC	-	Power supply +5V
32	MDSPIN	I	Data input for DSP	63	MLPSEL0	O	Master clock switch output of DSP
33	MDSPCK	O	Clock signal output for DSP	64	VSS	-	Connect to ground

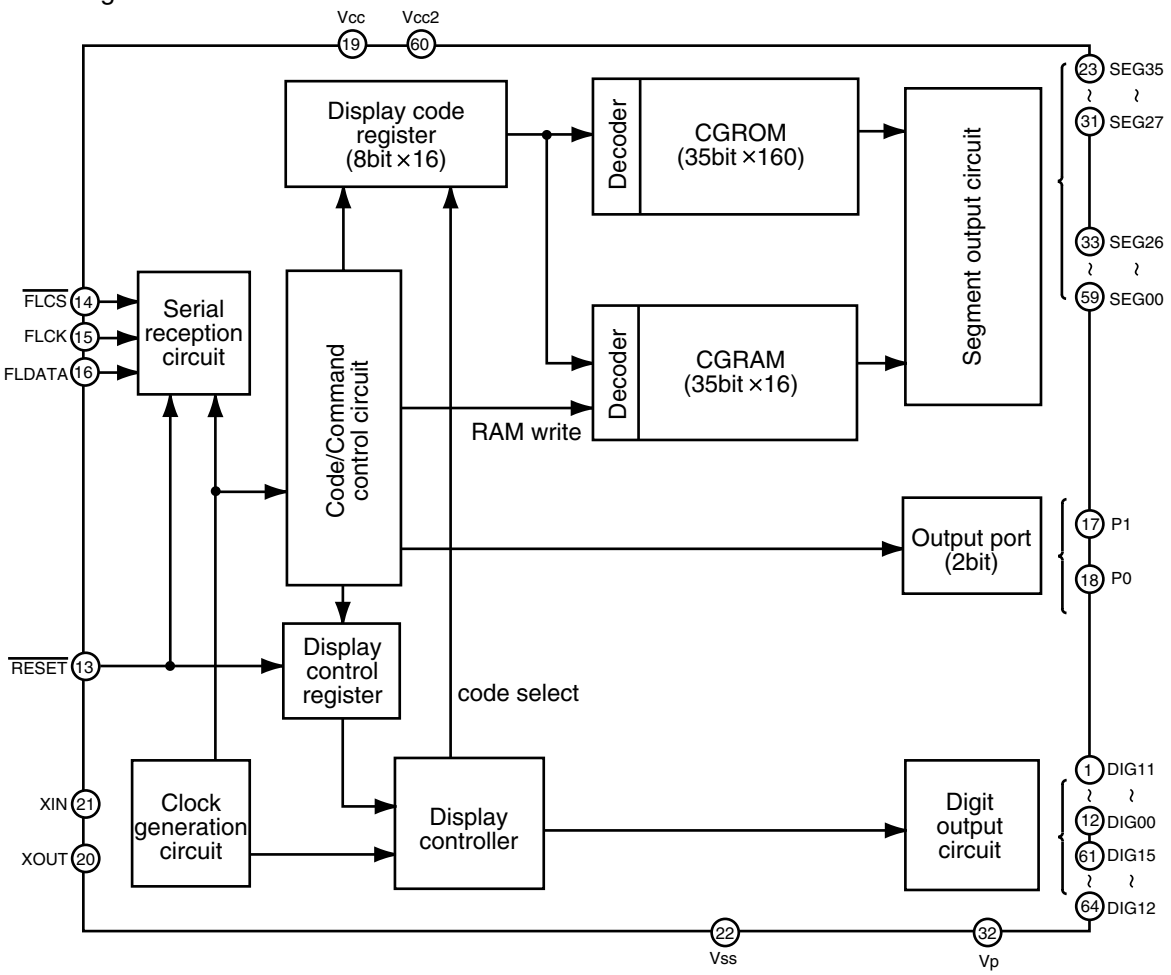
3.Pin Function (2/2)

M30622EC-FP

Pin No.	Symbol	I/O	Function
65	K2LATCH	O	Latch output for K2
66	PLLSEL1	O	Switch output for PLL
67	PLLSEL0	O	Switch output for PLL
68	LMUTE	O	Sub woofer mute output
69	CMUTE	O	Center mute output
70	SMUTE	O	Surround mute output
71	FMUTE	O	Front mute output
72	K2SCK	O	Clock signal output for K2
73	K2DATA	O	Data output for K2
74	K2CS	O	Chip select output to K2
75	FLCS	O	Chip select output for FL driver
76	FLPOR	O	Reset signal output for FL driver
77	STANDBYIND	O	STANDBY indicator control signal output
78	AUDIOIND	O	AUDIO indicator control signal output
79	PROGSCL	O	Clock signal output for progressive
80	PROGSDA	O	Data output for progressive
81	PROGPWA	O	ON/OFF output for progressive
82	PROGRST	O	Reset signal output for progressive
83	D60P60I	O	D terminal control signal output
84	DOUT1	O	D terminal aspect ratio output
85	DOUT2	O	D terminal aspect ratio output
86	KEYO2	O	Key matrix output 2
87	KEYO1	O	Key matrix output 1
88	KEYO0	O	Key matrix output 0
89	KEYI2	I	Key matrix input 2
90	KEYI1	I	Key matrix input 1
91	KEYI0	I	Key matrix input 0
92	DEVIDE-MCK	O	Clock control output for DSP
93	AICCTRL	O	Clock control output for DSP
94	IECZIVA	O	Digital output control signal output
95	IECDSP	O	Digital output control signal output
96	AVSS	-	Connect to ground
97	VDFF	O	Control signal output for video power
98	VREF	I	Internal AD reference input
99	AVCC	-	Power supply +5V
100	GND	-	Connect to ground

■ M66004SP(IC802):FL DRIVER

1.Block diagram

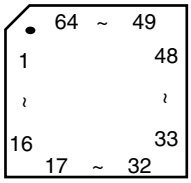


2.Pin function

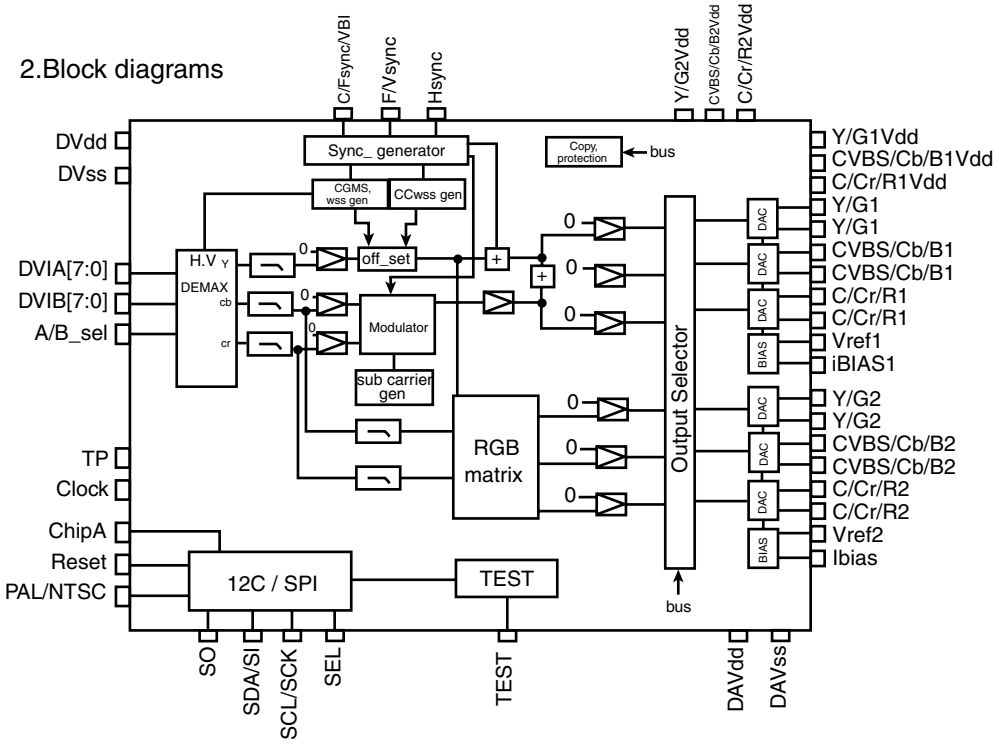
Pin.No.	Symbol	I/O	Function
1	D11	-	Non connect
2~12	D10~D0	O	FL digit control signal output.
13	POR	I	FL Driver chip select.
14	CS	I	Chip select signal input.
15	SCK	I	Shift clock signal input.
16	SDATA	I	Serial data input.
17	FLOFFIND	O	Indicator control signal output.
18	K2IND	O	Indicator control signal output.
19	VCC1	-	Power supply for internal logic.
20	XOUT	O	Clock signal output.
21	XIN	I	Clock signal input.
22	VSS	-	Connect to GND.
23	S35	-	Non connect.
24~31	S34~S27	O	FL Segment control signal output.
32	VP	-	Power supply.
33~59	S26~S0	O	FL Segment control signal output.
60	VCC2	-	Power supply for grid output and segment output.
61~64	D15~D12	-	Non connect

■ MC44724AVFU (IC554) : VIDEO ENCODER

1.Terminal layout



2.Block diagrams



3.Pin function

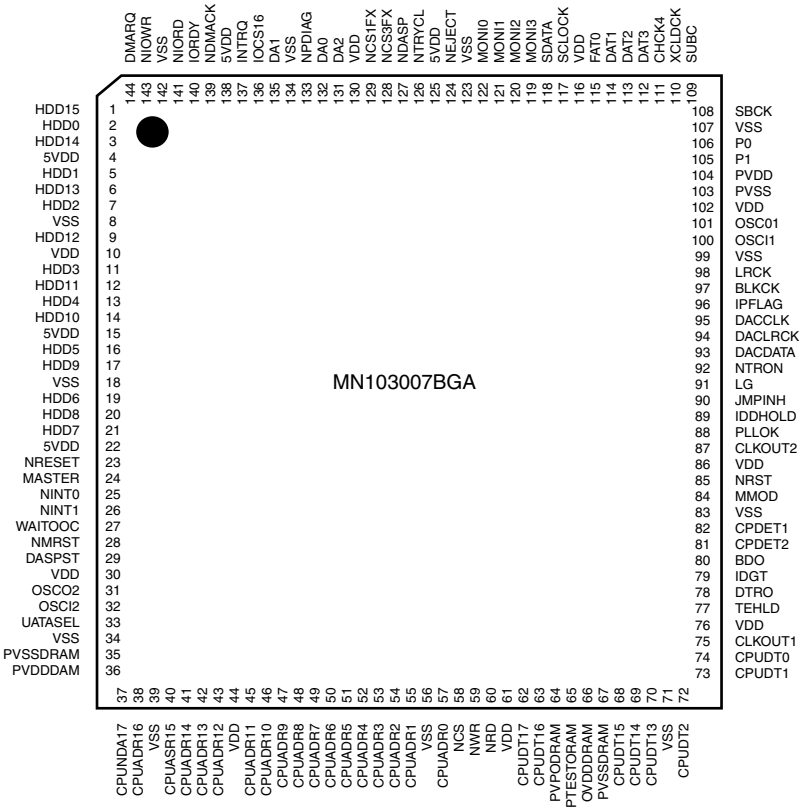
No.	Symbol	I/O	Function	No.	Symbol	I/O	Function
1	CVBS/Cb/B1	O	Analog composite drive signal (+)	33	SO	-	Non connect
2	$\overline{\text{CVBS/Cb/B1}}$	O	Analog composite drive signal (-)	34	SDA/SI	I	SPI Mode : Serial data input
3	CVBS/Cb/B1Vdd	-	Power supply for CVBS/Cb/B DAC1	35	SCL/SCK	I	Serial clock input
4	Y/G1	O	Analog brightness signal/G drive signal (+)	36	SEL	I	Power supply for serial data,chip select,digital
5	$\overline{\text{Y/G1}}$	O	Analog brightness signal/G drive signal (-)	37	DVdd	--	Power supply for digital circuit
6	Y/G1/Vdd	-	Power supply for Y/G DAC	38	DVss	--	Digital ground
7	C/Cr/R1	O	Analog chroma signal (+)	39	DVIN7	I/O	Y data input / test data I/O
8	$\overline{\text{C/Cr/R1}}$	O	Analog chroma signal (-)	40	DVIN6	I/O	Y data input / test data I/O
9	C/Cr/R1Vdd	-	Power supply for C/Cr/RDAC	41	DVIN5	I/O	Y data input / test data I/O
10	DAVss	-	Connect to ground for DAC	42	DVIN4	I/O	Y data input / test data I/O
11	TBIAS1	O	Standard BIAS for DAC1	43	DVIN3	I/O	Y data input / test data I/O
12	Vref1	-	Standard voltage for DAC1	44	DVIN2	I/O	Y data input / test data I/O
13	DAVdd	-	Power supply for DAC	45	DVIN1	I/O	Y data input / test data I/O
14	Vref2	-	Standard voltage for DAC2	46	DVIN0	I/O	Y data input / test data I/O
15	TBIAS2	O	Standard BIAS for DAC2	47	TVIN	I	VIDEO mute on Reset(0:nomal, 1:mute)
16	NC	-	Non connect	48	EXT	I/O	Frame output / VBI information input
17	CVBS/Cb/B2	O	Analog composite drive signal (+)	49	F/Vsyac	I/O	Frame / Vertical, synchronous I/O
18	CVBS/Cb/B2	O	Analog composite drive signal (-)	50	Chsyac	I/O	The horizontal, synchronous I/O
19	CVBS/Cb/B2Vdd	-	Power supply for CVBS/Cb/B DAC2	51	DATST	I	Data input
20	Y/G2	O	Analog brightness signal/G drive signal (+)	52	TP8	I/O	Multiplex data input
21	$\overline{\text{Y/G2}}$	O	Analog brightness signal/G drive signal (-)	53	TP7	I/O	Multiplex data input
22	Y/GVdd	-	Power supply for Y/G DAC	54	TP6	I/O	Multiplex data input
23	C/Cr/R2	O	Analog chroma signal (+)	55	TP5	I/O	Multiplex data input
24	$\overline{\text{C/Cr/R2}}$	O	Analog chroma signal (-)	56	DVss	-	Ground for digital circuit
25	C/Cr/R2Vdd	-	Power supply for C/Cr/RDAC2	57	DVdd	-	Power supply for digital circuit
26	ChipA	-	Chip address selection	58	TP4	I/O	Data input / Test data I/O
27	TEST	I	Connect to test pin	59	TP3	I/O	Data input / Test data I/O
28	DVdd	-	Digital ground	60	TP2	I/O	Data input / Test data I/O
29	CLOCK	I	Clock signal input (27MHz)	61	TP1	I/O	Data input / Test data I/O
30	DVss	-	Power supply for digital circuit	62	TP0	I/O	Data input / Test data I/O
31	Reset	I	Reset signal input L:ON	63	DLVdd	-	Power supply for D/A converter
32	PAL/NTSC	I	Selection NTSC/PAL NTSC:L PAL:H	64	DLVss	-	Ground for D/A converter

■ MN102LP25G(IC401):UNIT CPU

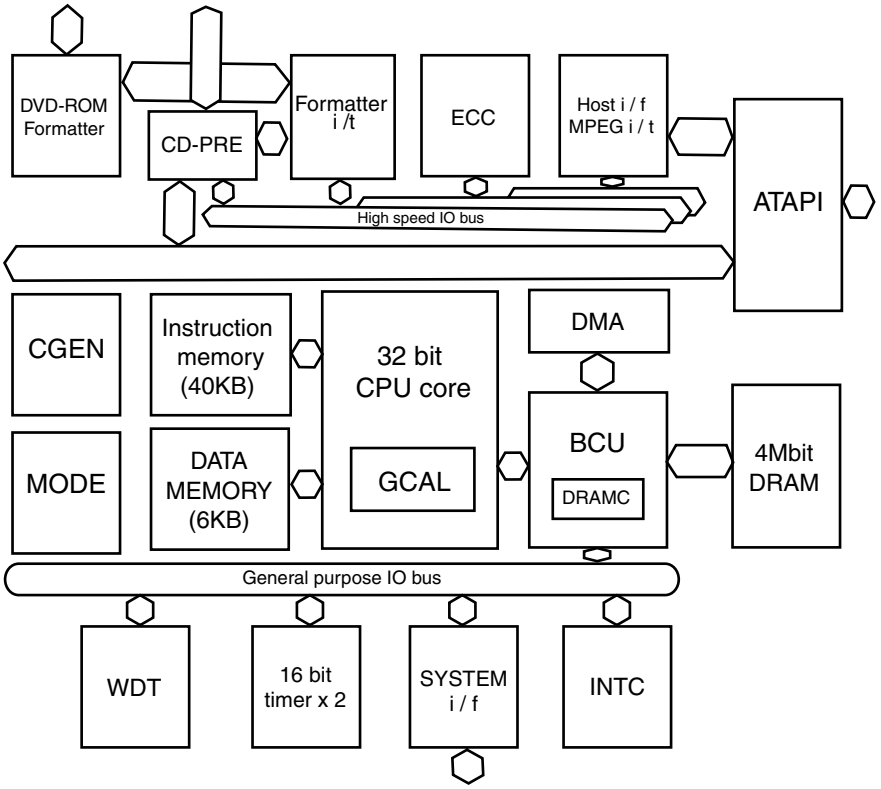
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	SWCLOSE	I	Detection switch of tray close
2	RE	O	Read enable	52	SWOPEN	I	Detection switch of tray open
3	MUTE	O	Driver mute	53	ADSCEN	O	Serial enable signal for ADSC
4	WEM	O	Write enable	54	VDD	-	Non connect
5	CS0	O	Non connect	55	EFPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for ZIVA	57	BUSY	I	Communication busy
8	CS3	O	Chip select for outer ROM	58	REQ	O	Communication Request
9	TCLOSE	O	Tray close signal output	59	CIRCEN	O	Serial I/F chip selection
10	TOPEN	O	Tray open signal output	60	TEHC	O	To front end processor
11	LSIRST	I	LSI reset	61	VSS	-	Power supply
12	WORD	O	Bus selection input	62	EECS	O	Chip select signal for EEPROM
13	A0	O	Address bus 0 for CPU	63	EECK	O	Clock signal for EEPROM
14	A1	O	Address bus 1 for CPU	64	EEDI	I	Input data for EEPROM
15	A2	O	Address bus 2 for CPU	65	EEDO	O	Output data for EEPROM
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLK0	I	Communication clock
18	SYSCLK	O	System clock signal output	68	S2UDT	I	Communication input data
19	VSS	-	Power supply	69	S2SDT	O	Communication output data
20	XI	-	Non connect	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Non connect	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input(13.5MHz)	73	-	-	Non connect
24	OSCO	-	Non connect	74	-	-	Non connect
25	MODE	I	CPU Mode selection input	75	NMI	-	Non connect
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	CSSIRQ	O	
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	Non connect
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	O	Address bus 18 for CPU	91	TEST8	I	Test signal 8 input
42	A19	O	Address bus 19 for CPU	92	VSS	-	Power supply
43	VSS	-	Power supply	93	D0	I/O	Data bus 0 of CPU
44	A20	O	Address bus 20 for CPU	94	D1	I/O	Data bus 1 of CPU
45	TXSEL	-	TX Select signal	95	D2	I/O	Data bus 2 of CPU
46	TMPSN	-	Connect to ground	96	D3	I/O	Data bus 3 of CPU
47	ADPD	-	Non connect	97	D4	I/O	Data bus 4 of CPU
48	-	-	Non connect	98	D5	I/O	Data bus 5 of CPU
49	-	-	Non connect	99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

■ MN103007BGA (IC301) : Optical disc controller

1.Pin layout



2.Block diagram



3.Pin function

MN103007BGA(1/2)

Pin NO.	Symbol	I/O	Function	Pin NO.	Symbol	I/O	Function
1	HDD15	I/O	ATAPI data	48	CPUADR8	I	System control address
2	HDD0	I/O	ATAPI data	49	CPUADR7	I	System control address
3	HDD14	I/O	ATAPI data	50	CPUADR6	I	System control address
4	5VDD			51	CPUADR5	I	System control address
5	HDD1	I/O	ATAPI data	52	CPUADR4	I	System control address
6	HDD13	I/O	ATAPI data	53	CPUADR3	I	System control address
7	HDD2	I/O	ATAPI data	54	CPUADR2	I	System control address
8	VSS			55	CPUADR1	I	System control address
9	HDD12	I/O	ATAPI data	56	VSS		GND
10	VDD			57	CPUADR0	I	System control address
11	HDD3	I/O	ATAPI data	58	NCS	I	System control chip selection
12	HDD11	I/O	ATAPI data	59	NWR	I	System control wright
13	HDD4	I/O	ATAPI data	60	NRD	I	System control lead
14	HDD10	I/O	ATAPI data	61	VDD		Apply 3V
15	5VDD			62	CPUDT7		System control data
16	HDD5	I/O	ATAPI data	63	CPUDT6		System control data
17	HDD9	I/O	ATAPI data	64	PVPPDRAM	O	C=10000PF is connected
18	VSS						between VSS
19	HDD6	I/O	ATAPI data	65	PTESTDRAM	I	VSS connected
20	HDD8	I/O	ATAPI data	66	OVDDDRAM		
21	HDD7	I/O	ATAPI data	67	PVSSDRAM		
22	5VDD			68	CPUDT5		System control data
23	NRESET	I	ATAPI reset	69	CPUDT4		System control data
24	MASTER	I/O	ATAPI master / slave selection	70	CPUDT3		System control data
25	NINT0	O	System control interruption 0	71	VSS		GND
26	NINT1	O	System control interruption 1	72	CPUDT2		System control data
27	WAITODC	O	System control weight control	73	CPUDT1	I/O	System control data
28	NMRST	O	System control reset	74	CPUDT0	I/O	System control data
29	DASPST	I	DASP signal initializing	75	CLKOUT1	O	16.9/11.2/8.45MHz clock
30	VDD			76	VDD	-	Apply 3V
31	OSCO2	I,O	VSS connection,OPEN	77	TEHLD	O	Mirror gate
32	OSCI2	I,O	VSS connection, OPEN	78	DTRO	O	Data part frequency control
33	UATASEL	I	VSS connection				switch
34	VSS			79	IDGT	O	Part CAPA switch
35	PVSSDRAM			80	BDO	I	RF dropout / BCA data of
36	PVDODRAM						making to binary
37	CPUADR17	I	System control address	81	CPDET2	I	Outer side CAPA detection
38	CPUADR18	I	System control address	82	CPDET1	I	Side of surroundings on inside
39	VSS			83	VSS		GND
40	CPUADR15	I	System control address	84	MMOD	I	VSS connected
41	CPUADR14	I	System control address	85	NRST	I	System reset
42	CPUADR13	I	System control address	86	VDD	-	Apply 3V
43	CPUADR12	I	System control address	87	CLKOUT2	O	16.9MHz clock
44	VDD			88	PLLOK	O	Frame mark detection
45	CPUADR11	I	System control address	89	IDOHOLD	O	ID gate for tracking holding
46	CPUADR10	I	System control address	90	JMPINH	O	Jump prohibition
47	CPUADR9	I	System control address				

3.Pin function

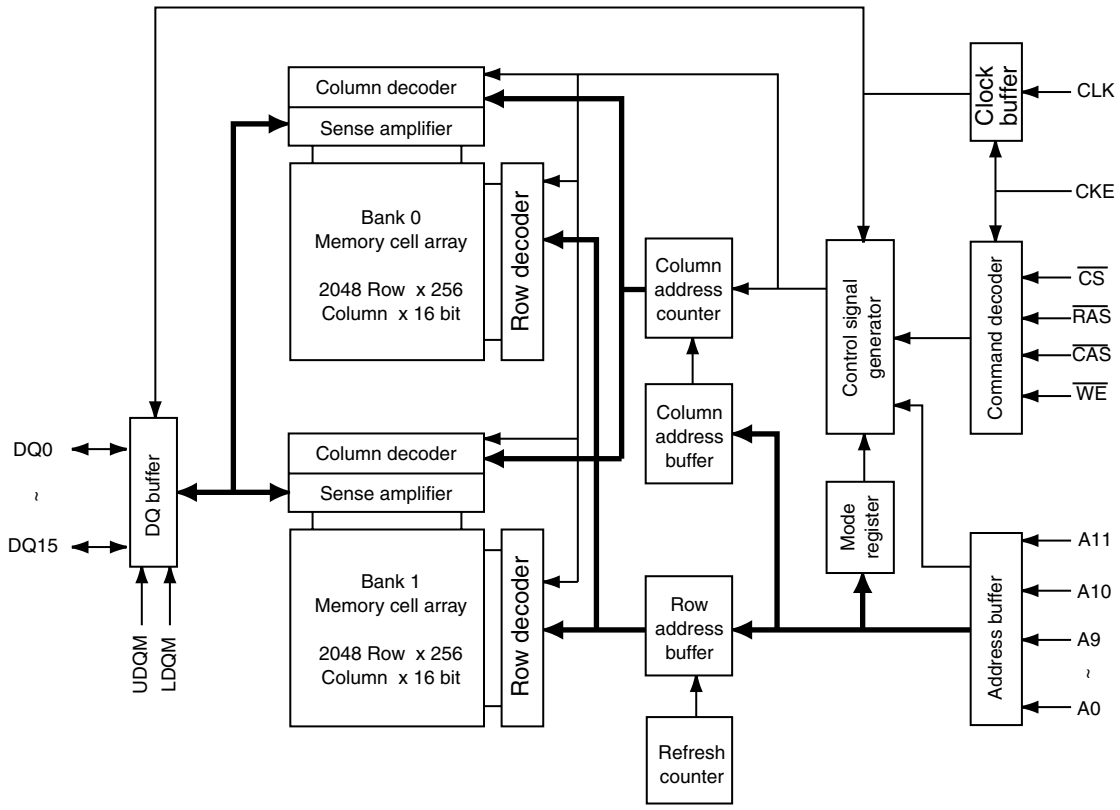
MN103007BGA(2/2)

Pin NO.	Symbol	I/O	Function
91	LG	O	Land / group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Cereal output
94	DACLRCK	O	L and R identification output
95	DACCLK	I	Clock for cereal output
96	IPFLAG	I	Interpolation flag input
97	BLKCK	I	Sub-code,Block clock input
98	LRCK	I	L and R identification signal output
99	VSS		
100	OSCI1	I,O	16.9MHz oscillation
101	OSCO1	I,O	16.9MHz oscillation
102	VDD		
103	PVSS		
104	PVDD		
105	P1	I/O	Terminal MASTER polarity switch input
106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input
107	VSS		
108	SBCK	O	Sub-code, Clock output for serial input
109	SUBC	I	Sub-code, Cereal input
110	XCLDCK	I	Sub-code, Frame clock input
111	CHCK4	I	Read clock to DAT3~0(Output of dividing frequency four from ADSC)
112	DAT3	I	Read data from DISC (Parallel output from ADSC)
113	DAT2	I	
114	DAT1	I	
115	DAT0	I	
116	VDD		
117	SCLOCK	I/O	Debugging cereal clock (270 Ω pull up)
118	SDATA	I/O	Debugging cereal data (270 Ω pull up)
119~122	MONI3~0	O	Internal goods title monitor
123	VSS		
124	NEJECT	I	Eject detection
125	5VDD		
126	NTRYCL	I	Tray close detection
127	NDASP	I/O	ATAPI Drive active/ Sulave connection I/O
128	NCS3FX	I	ATAPI host chip selection
129	NCS1FX	I	ATAPI host chip selection
130	VDD		
131	DA2	I/O	ATAPI host address
132	DA0	I/O	ATAPI host address

Pin NO.	Symbol	I/O	Function
133	NPDIAG	I/O	ATAPI slave master diagnosis input
134	VSS		
135	DA1	I/O	ATAPI host address
136	IOCS16	O	ATAPI output of selection of width of host data bus
137	INTRQ	O	ATAPI host interruption output
138	5VDD		
139	NDMACK	I	ATAPI host DMA response
140	IORDY	O	ATAPI host ready output
141	NIORD	I	ATAPI host read
142	VSS		
143	NIOWR	I/O	ATAPI host writes
144	DMARQ	O	ATAPI host DMA demand

■ MN4SV17160BT-10(IC504,IC505):16MB SDRAM

1.Block diagram

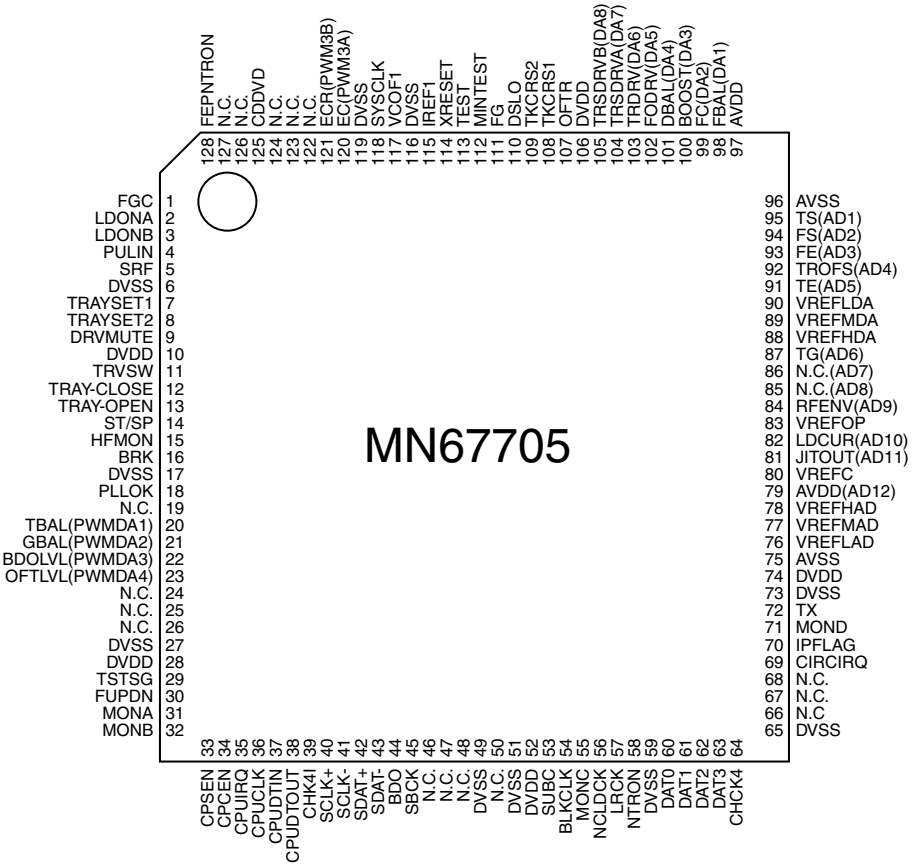


2.Pin function

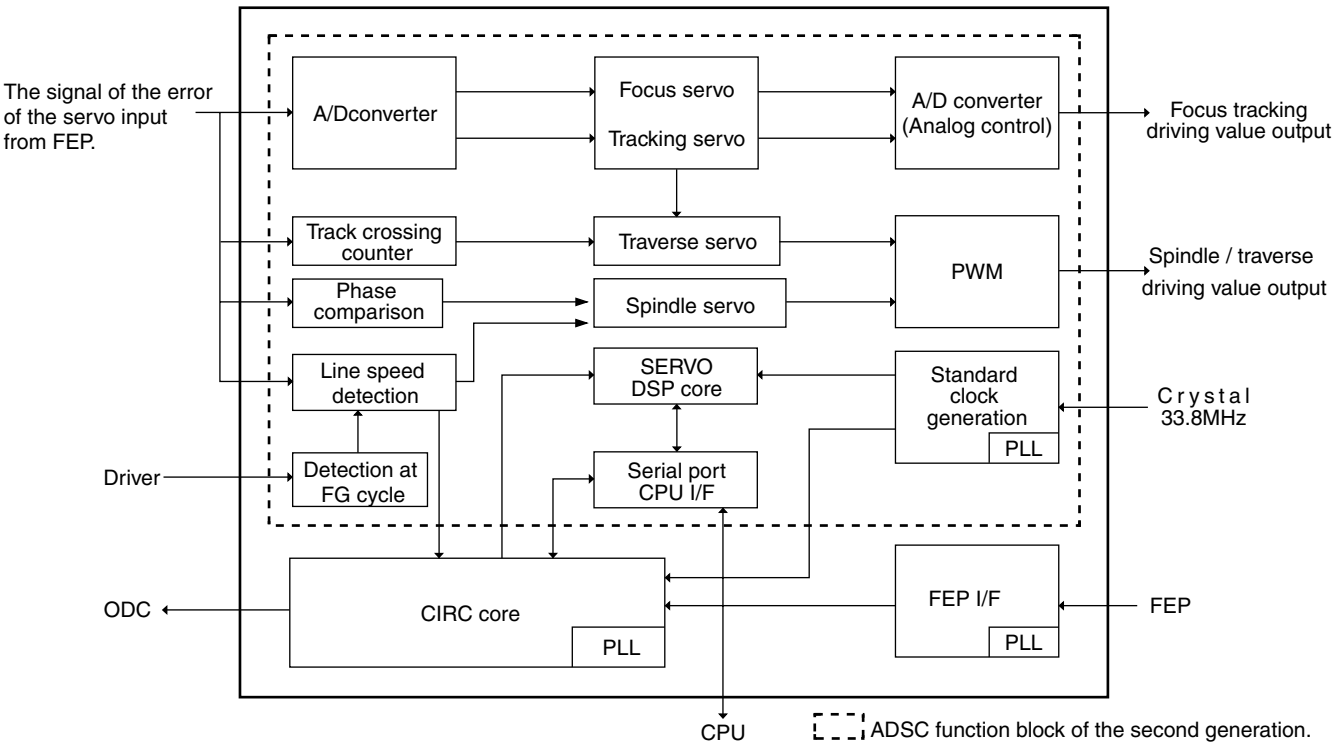
Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	VCC	Power supply	26	VSS	Connect to GND
2,3	DQ0,1	Data input/output	27~32	A4~9	Address inputs
4	VSS	Connect to GND	33	NC	Non connect
5,6	DQ2,3	Data input/output	34	CKE	Clock enable
7	VDD	Power supply	35	CLK	System clock input
8,9	DQ4,5	Data input/output	36	UDQM	Upper DQ mask enable
10	VSS	Connect to GND	37	NC	Non connect
11,12	DQ6,7	Data input/output	38	VCC	Power supply
13	VCC	Power supply	39,40	DQ8,9	Data input/output
14	LDQM	Lower DQ mask enable	41	VSS	Connect to GND
15	WE	Write enable	42,43	DQ10,11	Data input/output
16	CAS	Column address strobe	44	VDD	Power supply
17	RAS	Row address strobe	45,46	DQ12,13	Data input/output
18	CS	Chip enable	47	VSS	Connect to GND
19,20	A11,10	Address inputs	48,49	DQ14,15	Data input/output
21~24	A0~3	Address inputs	50	VSS	Connect to GND
25	VCC	Power supply			

■ MN67705EA(IC201):Digital servo controller

1.Pin layout



2.Block diagram



3.Pin function

MN67705EA (1/3)

Pin No.	Symbol	I/O	Function
1	FGC	0	H fixation
2	LDONA	O	Laser drive controlA (ON / OFF)
3	LDONB	O	Laser drive controlB (ON / OFF)
4	PULIN	O	DSL and PLL high boost signal (FEP)
5	SRF	O	Head amplifier gain H/L selection
6	DVSS	—	Ground for digital circuit
7	TRAYSET1	O	Tray drive ON/OFF and direction control
8	TRAYSET2	O	Tray drive ON/OFF and direction control
9	DRVMUTE	O	Drive IC mute control
10	DVDD	—	Power supply for digital circuit
11	TRVSW	I	Surroundings position detection in traverse
12	TRAY-CLOSE	I	Tray close detection SW
13	TRAY-OPEN	I	Tray opening detection SW
14	ST/SP	O	Spindle motor drive switch (START /STOP)
15	HFMON	O	High cycle module control
16	BRK	O	Spindle motor IC short brake control
17	DVSS	—	Ground for digital circuit
18	PLLOK	I	SYNC detection (DVD : 18T / CD : 22T)
19	N.C.	O	Non connect
20	TBAL(PWMDA1)	O	Tracking balance (FEP)
21	GBAL(PWMDA2)	O	Tangential balance (FEP)
22	BDOLVL(PWMDA3)	O	BDO slice level (FEP)
23	OFTLVL(PWMDA4)	O	Off-track error slice level (FEP)
24	N.C.	-	Non connect
25	N.C.	-	Non connect
26	N.C.	-	Non connect
27	DVSS	—	Ground for digital circuit
28	DVDD	—	Power supply for digital circuit
29	TSTSG	O	Self calibration signal (FEP)
30	FUPDN	O	Signal of frequency UP/DOWN of PLL (FEP)
31	MONA	O	Monitor terminal A
32	MONB	O	Monitor terminal B
33	CPSEN	I	Servo DSP cereal I/F chip selection (SYSCOM)
34	CPCEN	I	CIRC cereal I/F chip selection (SYSCOM)
35	CPUIRQ	O	Interrupt request to silicon (SYSCOM)
36	CPUCLK	I	Silicon cereal I/F clock (SYSCOM)
37	CPUDTIN	I	Silicon cereal I/F data input (SYSCOM)
38	CPUDTOUT	O	Silicon cereal I/F data output (SYSCOM)
39	CHK4I	I	Connects with unused DVSS
40	SCLK+	I	Lead channel clock differential motion signal (positive)
41	SCLK-	I	Lead channel clock differential motion signal (negative)
42	SDAT+	I	Lead channel data differential motion signal (positive)
43	SDAT-	I	Lead channel data differential motion signal (negative)
44	BDO	I	BDO + BCA (FEP)
45	SBCK	I	CD sub-code data shift clock (ODC)
46	IREF2	—	Connects with unused DVSS

3.Pin function

MN67705EA (2/3)

Pin No.	Symbol	I/O	Function
47	IREF3	—	Connects with unused DVSS
48	VCOF2	—	Connects with unused DVSS
49	DVSS	—	Ground for digital circuit
50	VCOE3	—	Connects with unused DVSS
51	DVSS	—	Ground for digital cirucuit
52	DVDD	—	Power supply for digital cirucuit
53	SUBC	O	CD sub-code (ODC)
54	BLKCLK	O	CD sub-code synchronous signal (ODC)/Jump output of one at DVD
55	MONC	O	Monitor terminal C
56	NCLDCK	O	Sub-code data frame clock (ODC)
57	LRCK	O	LR channel data strobe clock (ODC)
58	NTRON	O	L: Tracking ON (ODC)
59	DVSS	—	Ground for digital cirucuit
60	DAT0	O	CIRC / Binary making DVD data output
61	DAT1	O	CIRC / Binary making DVD data output
62	DAT2	O	CIRC / Binary making DVD data output
63	DAT3	O	CIRC / Binary making DVD data output
64	CHCK4	O	Synchronous clock of DAT0～3
65	DVSS	—	Ground for digital circuit
66	DACCLK	O	
67	DACLRCK	I	Connects with unused DVSS
68	DACDATA	I	Connects with unused DVSS
69	CIRCIRQ	O	RAM with built-in CIRC exceeds / Underflow interrupt
70	IPFLAG	O	CIRC error flag
71	MOND	O	Monitor terminal D
72	TX	O	Digital audio interface
73	DVSS	—	Ground for digital cirucuit
74	DVDD	—	Power supply for digital cirucuit
75	AVSS	—	Ground for analog cirucuit
76	VREFLAD	—	AD subordinate position standard voltage (0.6±0.1v)
77	VREFMAD	—	It is a place standard voltage in AD (1.4±0.1V)
78	VREFHAD	—	High-ranking AD standard voltage (2.2±0.1V)
79	AVDD	—	Power supply for analog circuit
80	VREFC(AD12)	I	
81	JIOUT(AD11)	I	Jitter signal(FEP)
82	LDCUR(AD10)	I	Laser drive current signal
83	VREFOP	—	Operation amplifier standard voltage(VREFC)
84	RFENV(AD9)	I	RFENV(FEP)
85	N.C.(AD8)	I	Connects with VREFC
86	N.C.(AD7)	I	Connects with VREFC
87	TG(AD6)	I	Tangential Phase difference (FEP)
88	VREFHDA	—	High-ranking AD standard voltage (2.2±0.1V)
89	VREFMDA	—	It is a place standard voltage in AD (1.4±0.1V)
90	VREFLDA	—	AD subordinate position standard voltage (0.6±0.1v)
91	TE(AD5)	I	Tracking error (FEP)
92	TROFS(AD4)	I	Tracking drive IC input offset
93	FE(AD3)	I	Focus error (FEP)

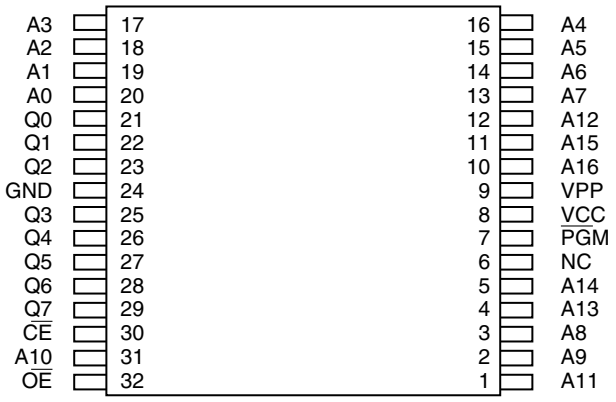
3.Pin function

MN67705EA(3/3)

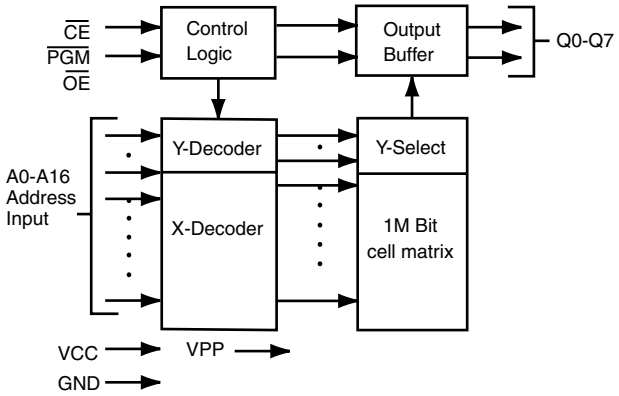
Pin No.	Symbol	I/O	Function
94	FS(AD2)	I	FS (FEP)
95	TS(AD1)	I	TS (FEP)
96	AVSS	—	Ground for analog circuit
97	AVDD	—	Power supply for analog circuit
98	FBAL(DA1)	O	Focus balance(FEP)
99	FC(DA2)	O	Cutting off frequency (FEP)
100	BOOST(DA3)	O	Amount of boost (FEP)
101	TBAL(DA4)	O	DSL offset balance (FEP)
102	FODRV(DA5)	O	Focus drive
103	TRDRV(DA6)	O	Tracking drive
104	TRSDRVA(DA7)	O	Traverse drive A aspect
105	TRSDRVB(DA8)	O	Traverse drive B aspect
106	DVDD	—	Power supply for digital circuit
107	OFTR	I	Off-track error signal (FEP)
108	TKCRS1	I	Track crossing signal 1 (FEP)
109	TKCRS2	I	Track crossing signal 2 (FEP)
110	DSLO	I	Binary making data slice signal (FEP)
111	FG	I	FG signal input (spindle motor driver)
112	MINTEST	—	Connects with DVSS
113	TEST	—	Connects with DVSS
114	XRESET	I	Reset L : Reset
115	IREF1	—	VCO reference current 1(for SYSCLK)
116	DVSS	—	Ground for digital circuit)
117	VCOF1	—	VCO control voltage 1 (for SYSCLK)
118	SYSCLK	I	33.8MHz system clock input
119	DVSS	—	Ground for digital circuit
120	EC(PWM3A)	O	Spindle motor drive
121	ECR(PWM3B)	O	
122	N.C.(PWM3A)	O	
123	N.C.(PWM2B)	O	
124	N.C.(PWM1A)	O	
125	CDDVD	O	CD/DVD control signal (FEP) CD : H DVD : L
126	N.C.(PWM0A)	O	
127	N.C.(PWM0B)	O	
128	FEPNTRON	O	Tracking ON (FEP)

■ MX27L1000TC-15(IC172,IC162):PROM

1.Pin layout



2. Block diagram

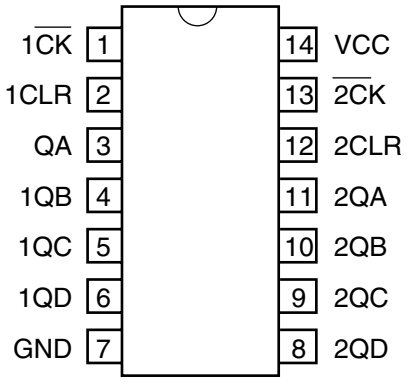


3.Pin function

Symbol	Description
A0-A16	Address input
Q0-Q7	Data input/output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{PGM}$	Write enable input
VPP	Power supply (write)
NC	Non connect
VCC	Power supply (+5V)
GND	Connect to ground

■ TC74AC393FT-X(IC715) : Dual binary counter

1.Pin layout



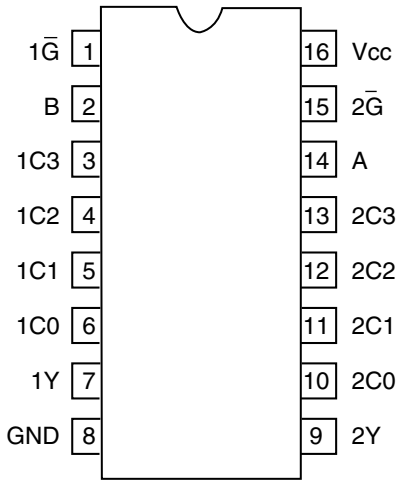
2.Truth table

INPUTS		OUTPUTS			
$\overline{CK}$	CLR	D	CK	Q	$\overline{Q}$
X	H	L	L	L	L
↓	L	COUNT UP			
↑	L	NO CHANGE			

X : Don't Care

■ TC74ACT153F-X(IC183):Dual 4-channel multiplexer

1.Pin layout



(TOP VIEW)

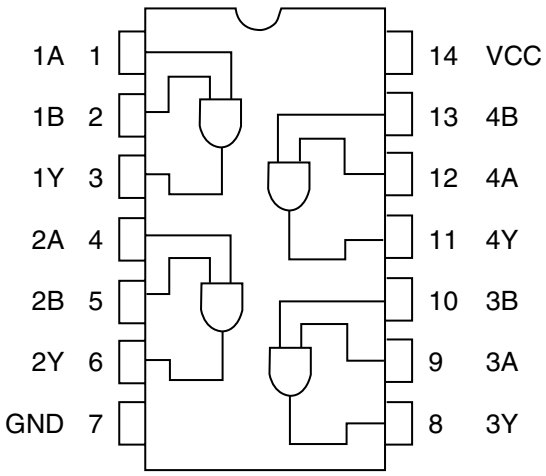
2.Truth table

SELECT INPUTS		DATA INPUTS				STORE	OUTPUT
B	A	C0	C1	C2	C3	$\bar{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

X:Don't Care

■ TC74HC08AP(IC915) / TC74HCT08AP(IC916):2-input and gate
TC74VHC08FT-X(IC722) / TC74VHCT08AFT-X(IC721):2-input and gate

1.Pin layout



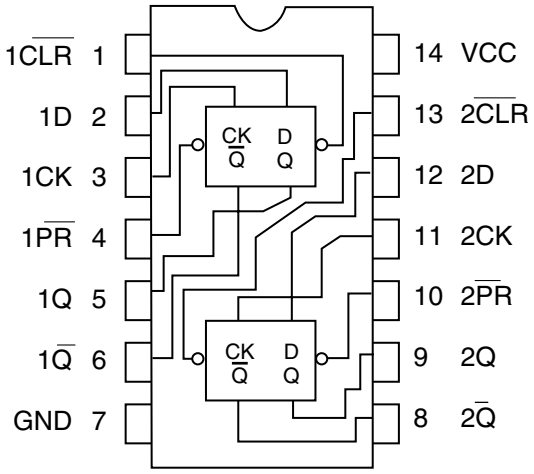
(TOP VIEW)

2.Truth table

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

■ TC74HC74AF-W(IC181):Dual D-type flip flop preset and clear
TC74VHC74FT-X (IC726,IC725)

1.Pin layout



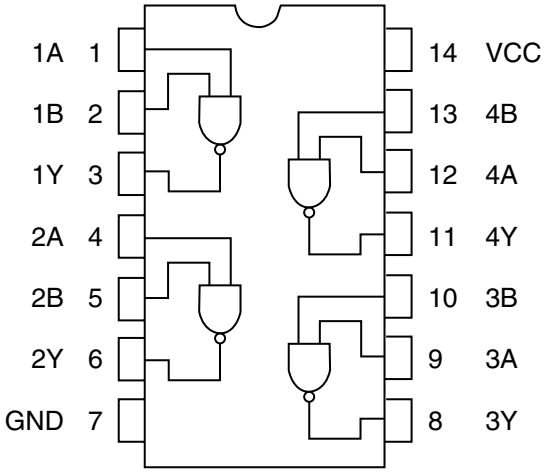
2.Truth table

INPUTS				OUTPUTS		FUNCTION
CLR	PR	D	CK	Q	Q	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	——
H	H	L	↑	L	H	——
H	H	H	↑	H	L	——
H	H	X	↓	Qn	Qn	NO CHANGE

X : Don't Care

■ TC74VHC03F-X(IC182):2-input nand gate

1.Pin layout



(TOP VIEW)

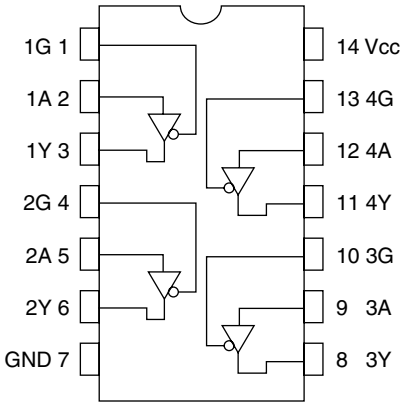
2.Truth table

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	L	Z
H	H	L

L : High impedance

■ TC74VHC125FT-X (IC557,IC558,IC559) : Buffer

1. Pin layout & block diagram



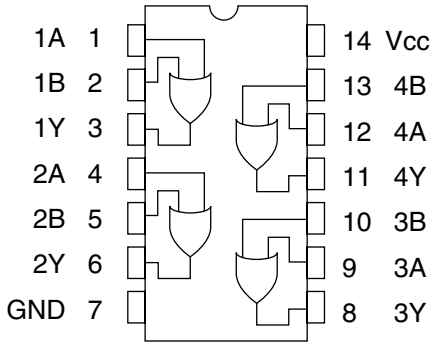
2. Truth table

INPUTS		OUTPUTS
G	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't care
Z:High impedance

■ TC74VHCT32AF-X (IC723) : Buffer

1. Pin layout

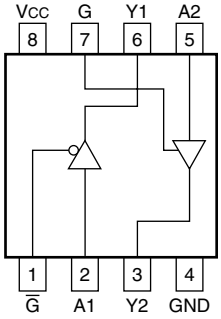


2.Truth table

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

■ TC7WH241FU-X (IC724): Dual bus buffer

1.Block diagram



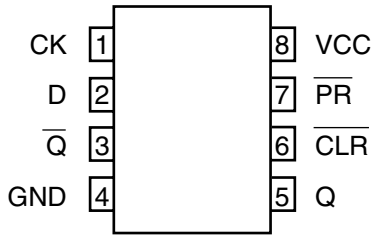
2. Truth table

INPUTS			OUTPUTS
$\overline{G}$	G	A	Y
L	H	L	L
L	H	H	H
H	L	X	Z

X: Don't care
Z:High impedance

■ TC7WH74FU-X(IC713,IC716) : Clock buffer

1.Pin layout



2.Truth table

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	——
H	H	L	↑	L	H	——
H	H	H	↑	H	L	——
H	H	X	↓	Qn	$\overline{Q}$n	NO CHANGE

X : Don't Care

■ XCF56362PV100(IC161,IC171):DSP

Pin Function (1/2)

Pin No.	Symbol	I/O	Function
1	SCK/SCL	I	SPI Serial clock / IC Serial clock
2	SS/HA2	I	SPI Slave select signal input / IC Slave address 2 input
3	HREQ	I/O	Host request signal input/output
4	SDO0	O	Serial data output 0
5	SDO1	O	Serial data output 1
6	SDO2/SDI3	I/O	Serial data output 2 / Serial data input 3
7	SDO3/SDI2	I/O	Serial data output 3 / Serial data input 2
8	VCCS	-	SHI,ESAI,DAX, and timer power supply terminal
9	GNDS	-	SHI,ESAI,DAX, and timer ground terminal
10	SDO4/SDI1	I/O	Serial data output 4 / Serial data input 1
11	SDO5/SDI0	I/O	Serial data output 5 / Serial data input 0
12	FST	I/O	Frame sync for transmitter
13	FSR	I/O	Frame sync for receiver
14	SCKT	I/O	Transmitter serial clock
15	SCKR	I/O	Receiver serial clock
16	HSCKT	-	Non connect
17	HSCKA	-	Non connect
18	VCCQL	-	Quiet core (low) power supply terminal
19	GNDQ	-	Quiet ground terminal
20	VCCQH	-	Quiet external (high) power supply terminal
21	HDS.HWR	I	Host data strobe / Host write data
22	HRW.HRD	I	Host read/write / Host read data
23	HACK.HRRD	I/O	Host acknowledge input / Receive host request output
24	HOREQ.HTRQ	O	Host request / Transmit host request
25	VCCS	-	SHI,ESAI,DAX, and timer power supply terminal
26	GNDS	-	SHI,ESAI,DAX, and timer ground terminal
27	ADO	O	Digital audio data output
28	ACI	I	Audio clock input
29	TIO0	I/O	Timer 0 schmitt-trigger input/output
30	HCS.HA10	I	Host chip select / Host address 10
31	HA2.HA9	I	Host address 2,9
32	HA1.HA8	I	Host address 1,8
33	HA0.HAS	I	Host address 0 / Host address strobe
34	H7.HAD7	I/O	Host data 7 / Host address 7
35	H6.HAD6	I/O	Host data 6 / Host address 6
36	H5.HDA5	I/O	Host data 5 / Host address 5
37	H4.HDA4	I/O	Host data 4 / Host address 4
38	VCCH	-	Host power supply terminal
39	GNDH	-	Host ground terminal
40	H3.HAD3	I/O	Host data 3 / Host address 3
41	H2.HAD2	I/O	Host data 2 / Host address 2
42	H1.HAD1	I/O	Host data 1 / Host address 1
43	H0.HAD0	I/O	Host data 0 / Host address 0
44	RESET	I	Reset signal input
45	VCCP	-	PLL Power supply terminal
46	PCAP	I	PLL Capacitor
47	GNDP	-	PLL Ground terminal

Pin Function (2/2) XCF56362PV100

Pin No.	Symbol	I/O	Function
48	GNDP1	-	PLL Ground 1 terminal
49	VCCQH	-	Quiet external (high) power supply terminal
50	AA3/RAS3	O	Address attribute or Row address strobe
51	AA2/RAS2	O	Address attribute or Row address strobe
52	CAS	O	Column address strobe
53	DE	I/O	Debug event
54	GNDQ	-	Quiet ground terminal
55	EXTAL	I	External clock input terminal
56	VCCQL	-	Quiet core (low) power supply terminal
57	VCCC	-	Bus control power supply terminal
58	GNDC	-	Bus control ground terminal
59	CLKOUT	O	Clock output terminal
60	NC	-	Non connect
61	PINIT/NMI	I	PLL Initial / Nonmaskable interrupt
62	TA	I	Transfer acknowledge terminal
63	BR	O	Bus request terminal
64	BB	I/O	Bus busy terminal
65	VCCC	-	Bus control power supply terminal
66	GNDC	-	Bus ground terminal
67	WR	O	Write enable signal output
68	RD	O	Read enable signal output
69	AA1/RAS1	O	Address attribute or row address strobe
70	AA0/RAS0	O	Address attribute or row address strobe
71	BG	I	Bus grant terminal
72	A0/RAS0	O	Address attribute or row address strobe
73	A1	O	Address bus terminal
74	VCCA	-	Address bus power supply terminal
75	GNDA	-	Address bus ground terminal
76~79	A2~A5	O	Address bus terminal
80	VCCA	-	Address bus power supply terminal
81	GNDA	-	Address bus ground terminal
82~85	A6~A9	O	Address bus terminal
86	VCCA	-	Address bus power supply terminal
87	GNDA	-	Address bus ground terminal
88,89	A10,A11	O	Address bus terminal
90	GNDQ	-	Quiet ground terminal
91	VCCQL	-	Quiet core (low) power supply terminal
92~94	A12~14	O	Address bus terminal
95	VCCQH	-	Quiet external (high) power supply terminal
96	GNDA	-	Address bus ground terminal
97~99	A15~A17	O	Address bus terminal
100~102	D0~2	I/O	Data bus terminal
103	VCCD	-	Data bus power supply terminal
104	GNDD	-	Data bus ground terminal
105~108	D3~D6	I/O	Data bus terminal

■ ZIVA3-PE0(IC501) : AV Decoder

ZIVA3-PEO (1/5)

Pin No.	Symbol	I/O	Function
1	PIO0	I/O	Programmable I/O pins.Input mode after reset.
2	HDATA0	I/O	8-bit bi-directional host data bus. writes data to the decoder Code FIFO via HDATA. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM via HDATA.
3	HDATA1		
4	HDATA2		
5	VDD-3.3	-	3.3-V supply voltage for I/O signals.
6	HDATA3	I/O	8-bit bi-directional host data bus. writes data to the decoder Code FIFO via HDATA. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM via HDATA.
7	VSS	-	Ground for core logic and I/O signals.
8	HDATA4	I/O	8-bit bi-directional host data bus. writes data to the decoder Code FIFO via HDATA. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM via HDATA.
9	HDATA5		
10	HDATA6		
11	HDATA7		
12	VDD-2.5	-	2.5-V supply voltage for core logic.
13	$\overline{\text{RESET}}$	I	Hardware reset. An external device asserts $\overline{\text{RESET}}$(active LOW) to execute a decoder hardware reset. To ensure proper initialization after power is stable,assert RESET for at least 20 ms.
14	VSS	-	Ground for core logic and I/O signals.
15	$\overline{\text{WAIT}}$/$\overline{\text{DTACK}}$	O	Transfer not complete / data acknowledge. Active LOW to indicate host initiated transfer is not complete.$\overline{\text{WAIT}}$ is asserted after the falling edge of $\overline{\text{CS}}$ and reasserted when decoder is ready to complete transfer cycle. Open drain signal, must be pulled-up via 1kW to 3.3 volts. Driven high for 10 ns before tristate.
16	$\overline{\text{INT}}$	O	Host interrupt. Open drain signal, must be pulled-up via 4.7kW to 3.3 volts. Driven high for 10 ns before tristate.
17	VDD-3.3	-	3.3-V supply voltage for I/O signals.
18	NC	O	No Connection
19	VSS	-	Ground for core logic and I/O signals.
20	NC	O	No Connection
21	PIO11	I/O	Programmable I/O pins. Input mode after reset
22	PIO12		
23	PIO13		
24	PIO14		
25	PIO15		
26	PIO16		
27	VDD-3.3	-	3.3-V supply voltage for I/O signals.
28	PIO17	I/O	Programmable I/O pins. Input mode after reset
29	VSS	-	Ground for core logic and I/O signals.
30	PIO18	I/O	Programmable I/O pins. Input mode after reset
31	PIO19	I/O	Programmable I/O pins. Output mode after reset
32	PIO20		
33	PIO21		
34	PIO22		
35	PIO23		
36	VDD-3.3	-	3.3-V supply voltage for I/O signals.
37	PIO24	I/O	Programmable I/O pins. Output mode after reset
38	VSS	-	Ground for core logic and I/O signals.
39	PIO25	I/O	Programmable I/O pins. Output mode after reset
40	VDD-2.5	-	2.5-V supply voltage for core logic.
41	PIO26	I/O	Programmable I/O pins. Output mode after reset
42	VSS	-	Ground for core logic and I/O signals.

ZIVA3-PEO (2/5)

Pin No.	Symbol	I/O	Function
44 45 46	PIO28 PIO29 PIO30	I/O	Programmable I/O pins. Output mode after reset
47	VDD-3.3	-	3.3-V supply voltage for I/O signals.
48	PIO31	I/O	Programmable I/O pins. Output mode after reset
49	VSS	-	Ground for core logic and I/O signals.
50 51	NC	O	No Connection
52	PIO1	I/O	Programmable I/O pins. Input mode after reset
53	MDATA15	I/O	Memory data
54	MDATA0	I/O	Memory data
55	VDD-3.3	-	3.3-V supply voltage for I/O signals.
56	MDATA14	I/O	Memory data.
57	VSS	-	Ground for core logic and I/O signals.
58 59 60	MDATA1 MDATA13 MDATA2	I/O	Memory data.
61	VDD-3.3	-	3.3-V supply voltage for I/O signals.
62	MDATA12	I/O	Memory data.
63	VSS	-	Ground for core logic and I/O signals.
64	MDATA3	I/O	Memory data.
65	VDD-2.5	-	2.5-V supply voltage for core logic.
66	MDATA11	I/O	Memory data.
67	VSS	-	Ground for core logic and I/O signals.
68	MDATA4	I/O	Memory data.
69	VDD-3.3	-	3.3-V supply voltage for I/O signals.
70	MDATA10	I/O	Memory data.
71	VSS	-	Ground for core logic and I/O signals.
72 73 74	MDATA5 MDATA9 MDATA6	I/O	Memory data.
75	VDD-3.3	-	3.3-V supply voltage for I/O signals.
76	MDATA8	I/O	Memory data.
77	VSS	-	Ground for core logic and I/O signals.
78	MDATA7	I/O	Memory data.
79	LDQM	O	SDRAM LDQM.
80	UDQM	O	SDRAM UDQM.
81	VDD-3.3	-	3.3-V supply voltage for I/O signals.
82	$\overline{\text{MWE}}$	O	SDRAM write enable. Decoder asserts active LOW to request a write operation to the SDRAM array.
83	VSS	-	Ground for core logic and I/O signals.
84	SD-CLK	O	SDRAM system clock.
85	$\overline{\text{SD-CAS}}$	O	Active LOW SDRAM column address.
86	$\overline{\text{SD-RAS}}$	O	Active LOW SDRAM row address.
87	VDD-3.3	-	3.3-V supply voltage for I/o signals.
88	$\overline{\text{SD-CS1}}$	O	Active LOW SDRAM bank select.
89	VSS	-	Ground for core logic and I/O signals.
90	SD-CS0	O	Active LOW SDRAM bank select.
91	VDD-2.5	-	2.5-V supply voltage for core logic.
92	NC	O	No Connection.
93	VSS	-	Ground for core logic and I/O signals.
94	NC	O	No Connection.
95	VDD-3.3	-	3.3-V supply voltage for I/O signals.
96	MADDR9	O	Memory address.
97	VSS	-	Ground for core logic and I/O signals.
98	MADDR11	O	Memory address.

ZIVA3-PEO (3/5)

Pin No.	Symbol	I/O	Function
99	MADDR8	O	Memory address.
100	MADDR10		
101	VDD-3.3	-	3.3-V supply voltage for I/O signals.
102	MADDR7	O	Memory address.
103	VSS	-	Ground for core logic and I/O signals.
104	MADDR0	O	Memory address.
105	MADDR6		
106	MADDR1		
107	VDD-3.3	-	3.3-V supply voltage for I/O signals.
108	MADDR5	O	Memory address.
109	VSS	-	Ground for core logic and I/O signals.
110	MADDR2	O	Memory address.
111	MADDR4		
112	MADDR3		
113	VDD-3.3	-	3.3-V supply voltage for I/O signals.
114	NC	O	No Connection
115	VSS	-	Ground for core logic and I/O signals.
116	NC	O	No Connection
117	VDD-2.5	-	2.5-V supply voltage for core logic.
118	NC	O	No Connection
119	VSS	-	Ground for core logic and I/O signals.
120	NC	O	No Connection
121			
122			
123	VDD-3.3	-	3.3-V supply voltage for I/O signals.
124	NC	O	No Connection
125	VSS	-	Ground for core logic and I/O signals.
126	NC	O	No Connection
127			
128	RESERVED	O	Open drain signal, must be pulled-up via 4.7kW to 3.3 volts.
129	PIO2	I/O	Programmable I/O pins. Input mode after reset.
130	NC	O	No Connection
131	RESERVED	I	Tie to VSS or VDD-3.3
132			
133	PIO3	I/O	Programmable I/O pins. Input mode after reset.
134	VDD-3.3	-	3.3-V supply voltage for I/O signals.
135	RESERVED	I	Tie to VSS or VDD-3.3
136	VSS	-	Ground for core logic and I/O signals.
137	RESERVED	I	Tie to VSS or VDD-3.3
138	PIO4	I/O	Programmable I/O pins. Input mode after reset.
139	RESERVED	I	Tie to VSS or VDD-3.3
140			
141	PIO5	I/O	Programmable I/O pins.Input mode after reset.
142	VDATA0	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
143	VDATA1		
144	VDD-2.5	-	2.5-V supply voltage for core logic.
145	VDATA2	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
146	VSS	-	Ground for core logic and I/O signals.
147	PIO6	I/O	Programmable I/O pins. Input mode after reset.
148	VDATA3	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA

ZIVA3-PEO (4/5)

Pin No.	Symbol	I/O	Function
149	VDD-3.3	-	3.3-V supply voltage for I/O signals.
150	VDATA4	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
151	VSS	-	Ground for core logic and I/O signals.
152	VDATA5	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
153	PIO7	I/O	Programmable I/O pins. input mode after reset.
154 155	VDATA6 VDATA7	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
156	PIO8	I/O	pins. Input mode after reset.
157	$\overline{\text{HSYNC}}$	I/O	Horizontal sync. The decoder begins outputting pixel data for a new horizontal line after the falling (active) edge of $\overline{\text{HSYNC}}$.
158	$\overline{\text{VSYNC}}$	I/O	Vertical sync.Bi-directional, the decoder outputs the top border of a new field on the first $\overline{\text{HSYNC}}$ after the falling edge of $\overline{\text{VSYNC}}$. $\overline{\text{VSYNC}}$ can accept vertical synchronization or top/bottom field notification from an external source. ($\overline{\text{VSYNC}}$ HIGH = bottom field. $\overline{\text{VSYNC}}$ LOW = Top field)
159	DA-IEC	O	Bitstream data in IEC-1937 or PCM data out in IEC-958 format.
160	VDD-3.3	-	3.3-V supply voltage for I/O signals.
161	DA-DATA0	O	PCM data out, eight channels. Serial audio samples relative to DA-BCK clock.
162	VSS	-	Ground for core logic and I/O signals.
163 164 165	DA-DATA1 DA-DATA2 DA-DATA3	O	PCM data out, eight channels. Serial audio samples relative to DA-BCK clock.
166	DA-LRCK	O	PCM left-right clock. Identifies the channel for each audio sample. the polarity is programmable.
167	DA-BCK	O	PCM bit clock. Divided by 8 from DA-XCK can be either 48 or 32 times the sampling clock.
168	VDD-2.5	-	2.5-V supply voltage for core logic.
169	DA-XCK	I/O	Audio master frequency clock. Used to generate DA-BCK and DA-LRCK. DA-XCK can be either 384 or 256 times the sampling frequency.
170	VSS	-	Ground for core logic and I/O signals.
171	DAI-DATA	I	PCM input data. two channels. Serial audio samples relative to DAI-BCK clock.
172	DAI-LRCK	I	PCM input left-right clock.
173	DAI-BCK	I	PCM input bit clock.
174	PIO9	I/O	Programmable I/O pins. Input mode after reset.
175	CLKSEL	I	Clock Select: Internal = VDD, External = VSS
176	A-VDD	-	3.3-V analog supply voltage.
177	VCLK	I	Video clock. Clocks out data on input. VDATA7.Clock is typically 27 MHz.
178	SYSCLK	I	System clock.Decoder requires external 27 MHz TTL oscillator. Drive with the same 27-MHz as VCK.
179	A-VSS	-	Analog ground for PLL
180	DVD-DATA0 /CD-DATA	I	Serial CD data. This pin is shared with DVD compressed data DVD-DATA0.
181	VDD-3.3	-	3.3-V supply voltage for I/O signals.
182	DVD-DATA1 /CD-LRCK	I	Programmable polarity 16-bit word synchronization to the decoder (right channel HIGH). This pin is shared with DVD compressed data DVD-DATA1.
183	VSS	-	Ground for core logic and I/O signals.
184	DVD-DATA2 /CD-BCK	I	CD bit clock. Decoder accept multiple BCK rates. This pin is shared with DVD compressed data DVD-DATA2.
185	DVD-DATA3 /CD-C2PO	I	Asserted HIGH indicates a corrupted byte.Decoder keeps the previous valid picture on-screen unit the next valid picture is decoded. This pin is shares with DVD compressed data DVD-DATA3.

ZIVA3-PEO (5/5)

Pin No.	Symbol	I/O	Function
186 187 188 189	DVD-DATA7 /CDG-SCLK DVD-DATA6 /CDG-SOS1 DVD-DATA5 /CDG-VFSY DVD-DATA4 /CDG-SDATA	I	DVD parallel compressed data from DVD DSP. When DVD DSP sends 32-bit words, it must write the MSB first. CDG-SDATA:CD+G (Sub code) Data.Indicates serial sub code data input. CDG-VSFY:CD+G (Sub code)Frame Sync. Indicates frame-start or composite synchronization input. CDG-SOS1:CD+G (Sub code) Block Sync.Indicates block-start synchronization input. CDG-SCLK: CD+G(Sub code)Clock. Indicates sub code data clock input or output.
190	PIO10	I/O	Programmable I/O pins. Input mode after reset.
191	VREQUEST	O	Video request. Decoder asserts VREQUEST to indicate that the video input buffer has available space.Polarity is programmable.
192	VSTROBE	I	Video strobe. Programmable dual mode pulse. Asynchronous and synchronous. In Asynchronous mode, an external source pulses VSTROBE to indicate data is ready for transfer. In synchronous mode VSTROBE clock data.
193	VDD-3.3	-	3.3-V supply voltage for I/O signals.
194	NC	O	No Connection
195	VSS	-	Ground for core logic and I/O signals.
196	V-DACK	I	In synchronous mode, Video data acknowledge. Asserted when DVD data is valid.Polarity is programmable.
197	VDD-2.5	-	2.5-V supply voltage for core logic.
198	RESERVED	I	Tie to VSS or VDD-3.3
199	VSS	-	Ground for core logic and I/O signals.
200	ERROR	I	Error in input data. If ERROR signal is not available from the DSP it must be grounded.
201	HOST8SEL	I	Always Ttie to VDD-3.3
202 203 204	HADDR0 HADDR1 HADDR2	I	Host address bus. 3-bit address bus selects one of eight host interface registers.
205	DTACKSEL	I	Tie HIGH to select $\overline{\text{WAIT}}$ signal, LOW to select $\overline{\text{DTACK}}$ signal (Motorola 68K mode).
206	$\overline{\text{CS}}$	I	Host chip select.Host asserts CS to select the decoder for a read or write operation.The falling edge of this signal triggers the read or write operation.
207	R/$\overline{\text{W}}$	I	Read/write strobe in M mode. write strobe in I mode.Host asserts R/$\overline{\text{W}}$ LOW to select write and LOW to select read.
208	$\overline{\text{RD}}$	I	Read strobe in I mode. Must be held HIGH in M Mode

JVC

VICTOR COMPANY OF JAPAN, LIMITED
PERSONAL & MOBILE NETWORK BUSINESS UNIT
1644, Shimotsuruma, Yamato, Kanagawa 242-8514, Japan

No.A0007

Printed in Japan
200104(S)